On Borrowed Time – Preventing Static Side-Channel Analysis

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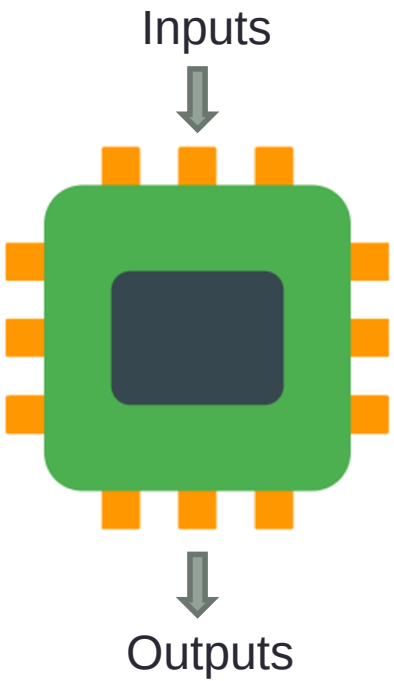
Also supported by CASA Cyber Security in the Age of Large-Scale Adversaries, Internet Society

Information leakage through physical side-channels



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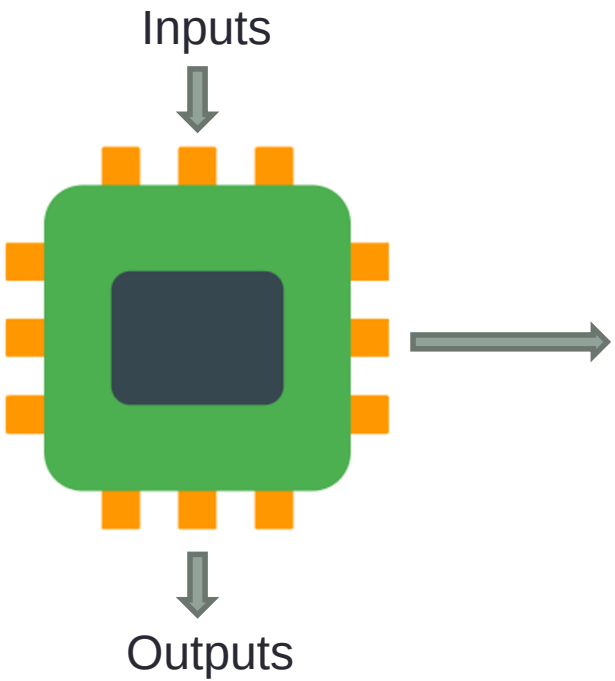

Environmental effects:

Power, Temperature, Acoustic, Electromagnetic

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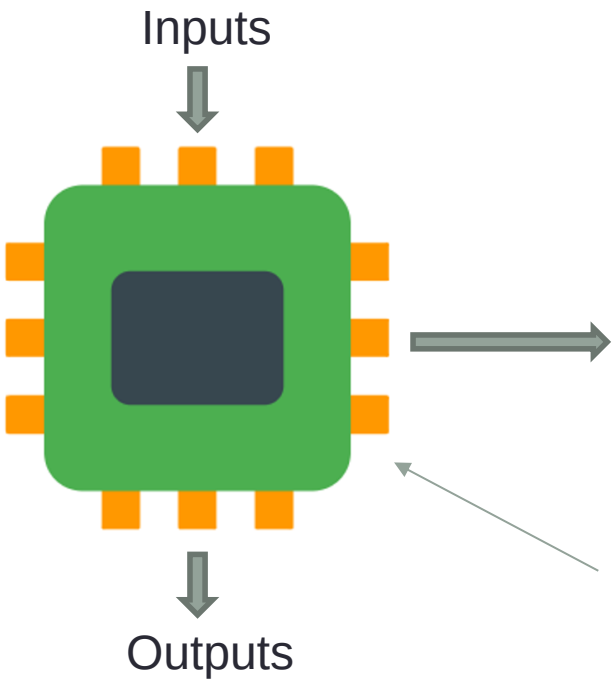

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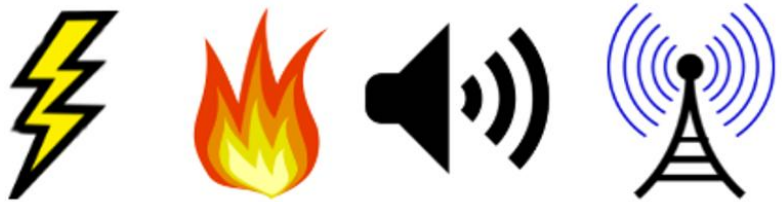

Black box model does not hold

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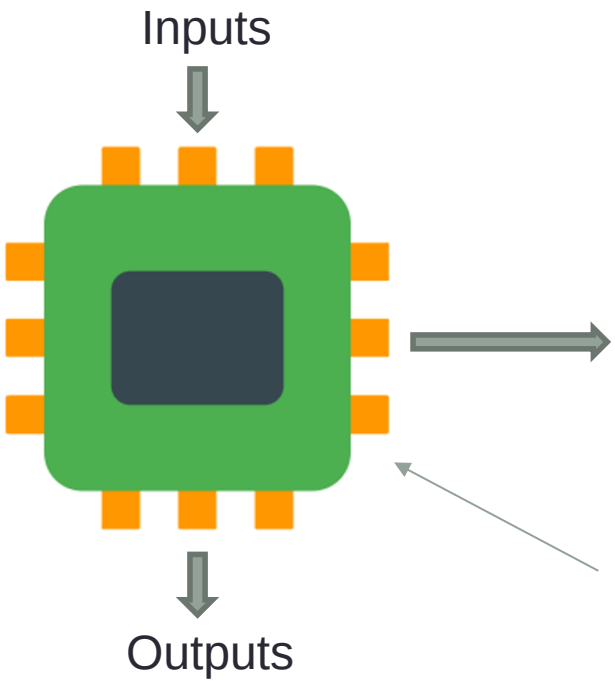

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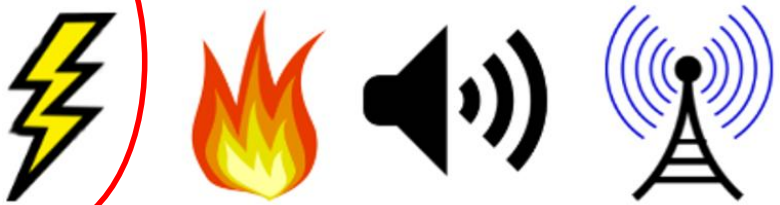

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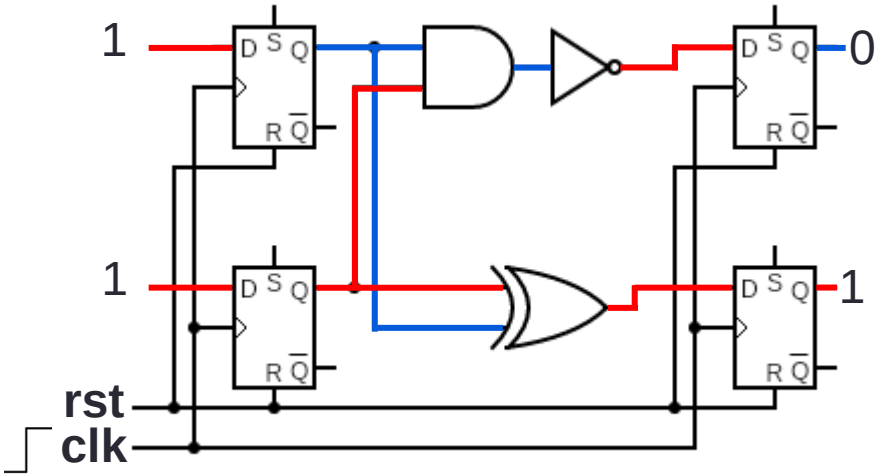
Power Analysis:
Static vs Dynamic Leakage Model



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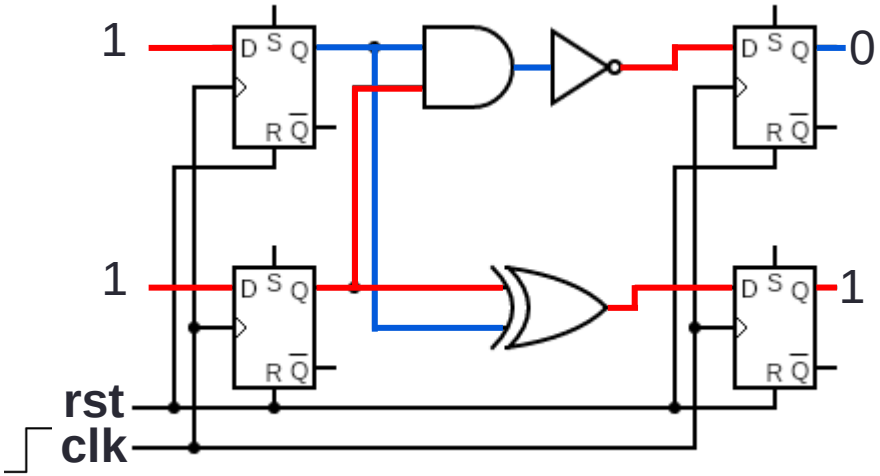

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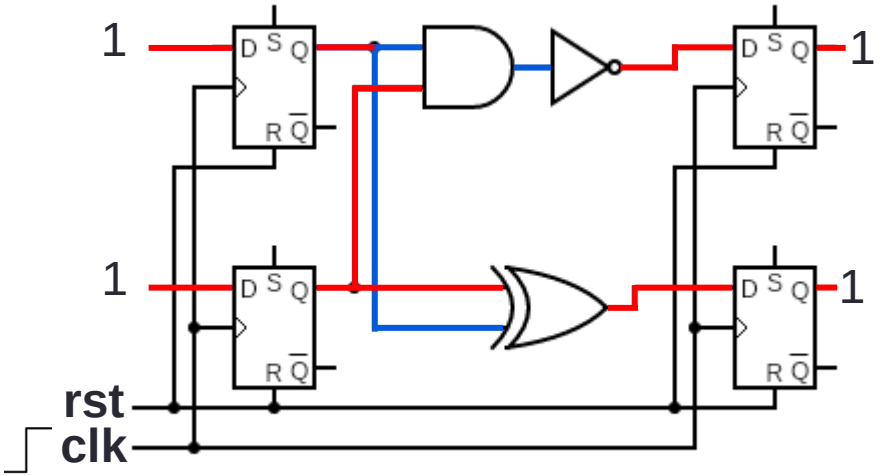

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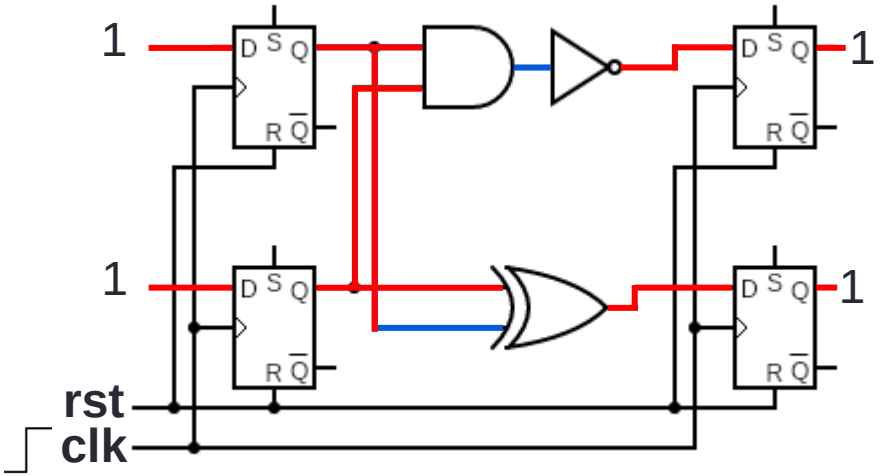

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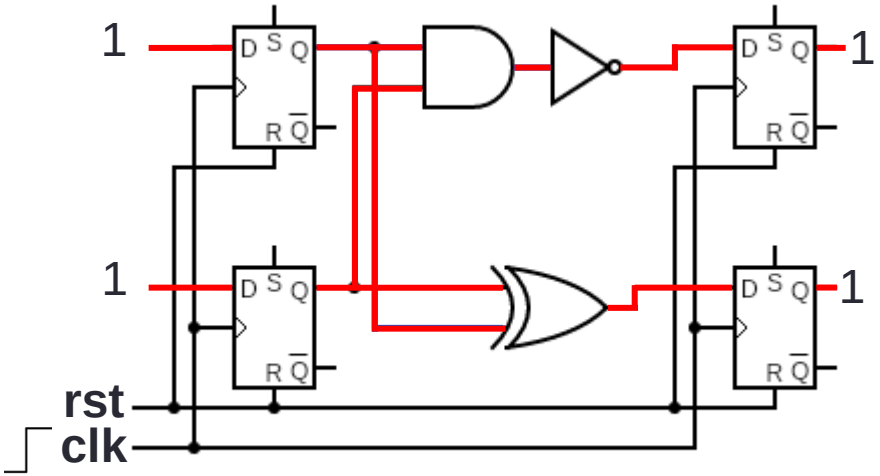

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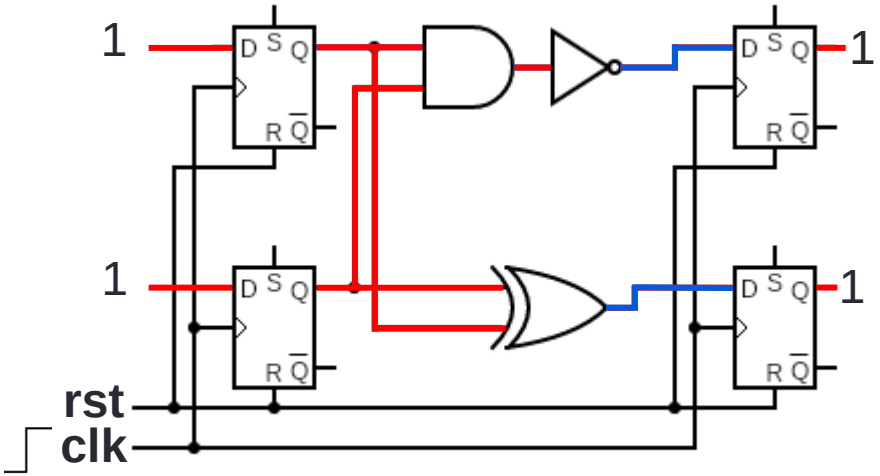

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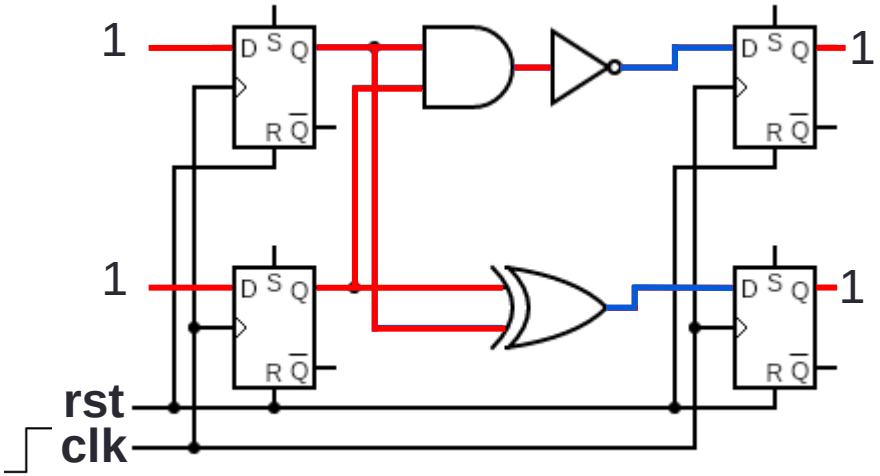
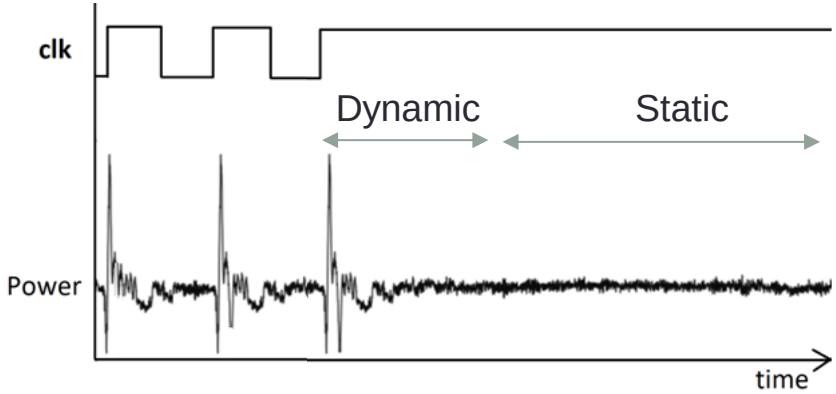
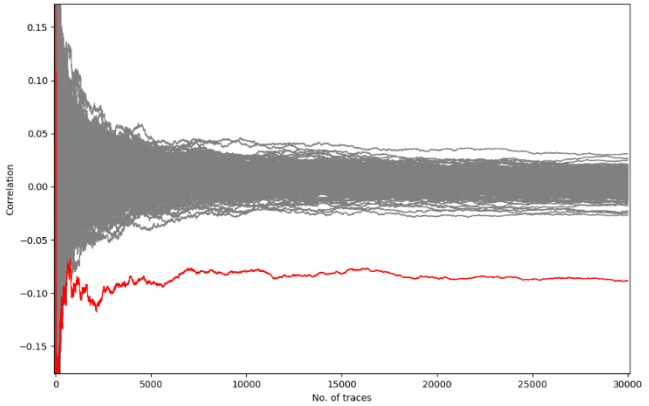


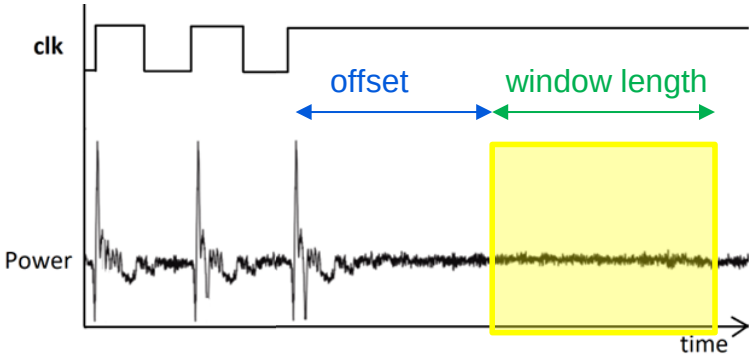


- Dynamic leakage comes from switching at clock transitions
- Static ‘steady-state’ leakage comes from values held in stateful elements

Determining the attack parameters

- We perform Correlation Power Analysis (CPA) on an AES FPGA implementation
- With a 20ms wait time (offset) and window length, we can recover the full key with 1,500 MTD





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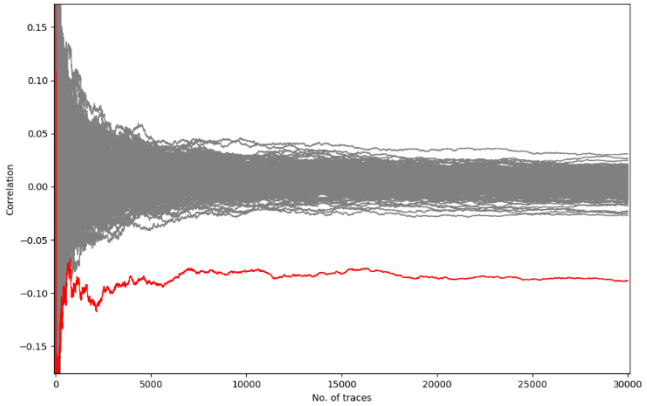
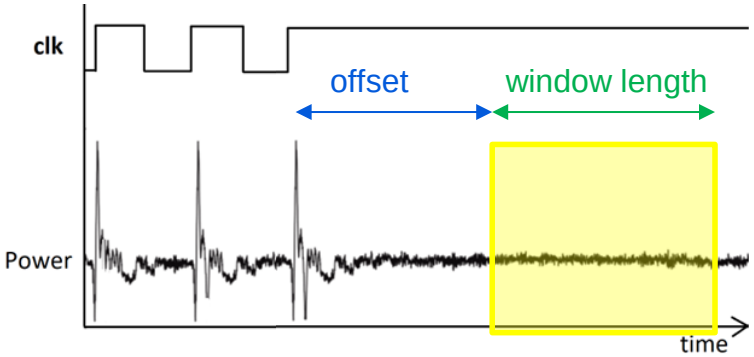
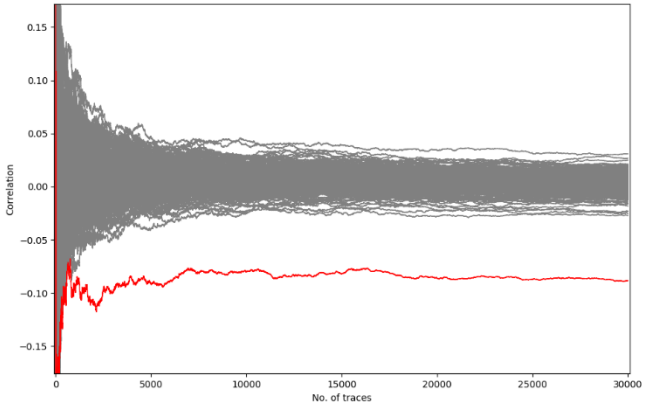
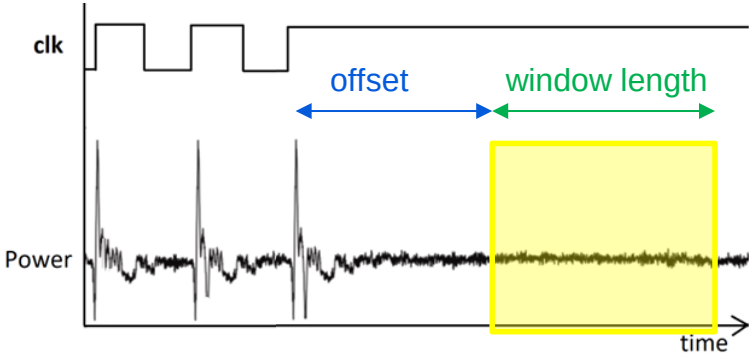


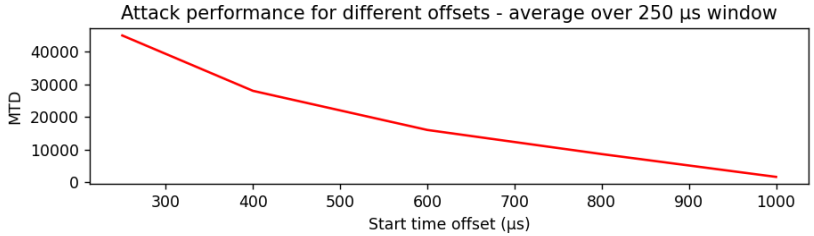


Determining the attack parameters

- We perform Correlation Power Analysis (CPA) on an AES FPGA implementation
- With a 20ms wait time (offset) and window length, we can recover the full key with 1,500 MTD
- We reduce the offset and window length
- No leakage for over 1 million traces at **200µs offset**



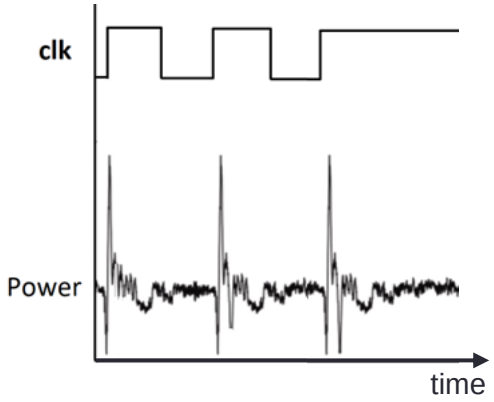




Borrowed Time countermeasure

Two conditions must hold within a target for static attack:

- The clock must be stopped
- Sensitive content must be retained in registers



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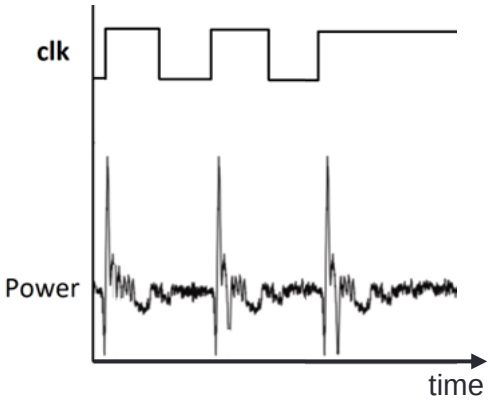

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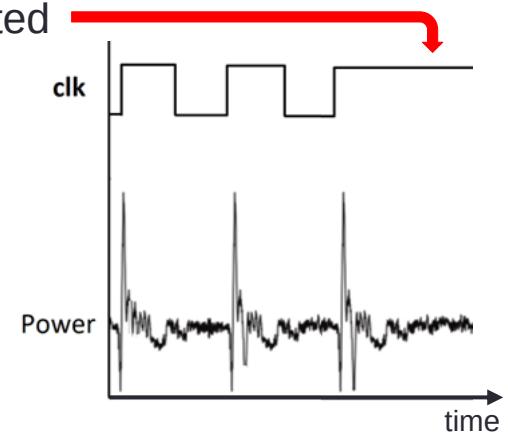
Protection: prevent these simultaneous conditions

Stopped clock detected

1



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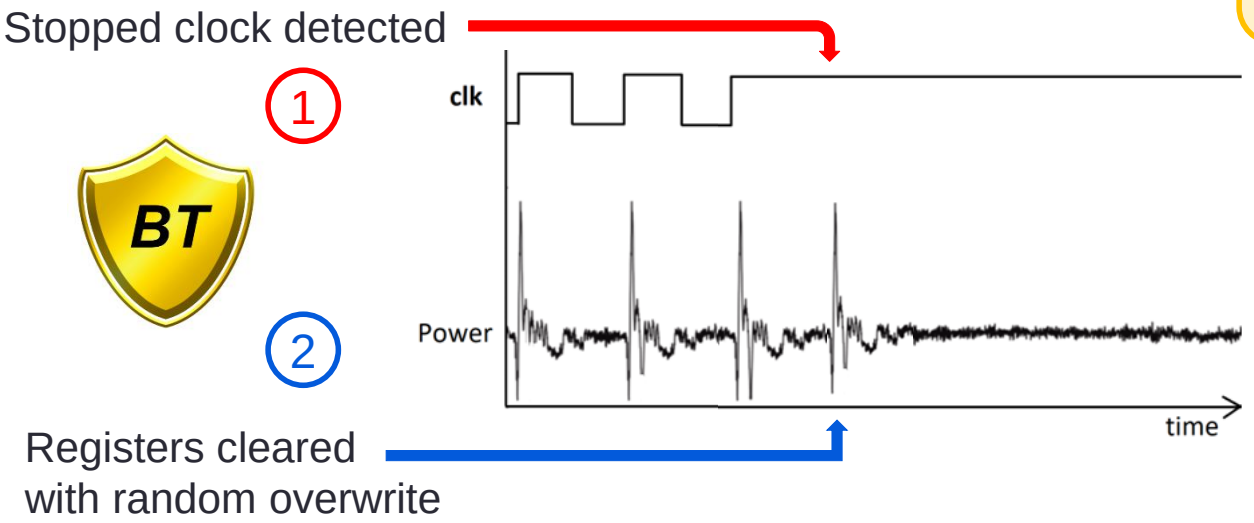

Borrowed Time variants

Two clock sensor primitives:

PLL-based

- Maintain internal oscillator and use this to check external clock source

Delay-chain-based

- Use asynchronous circuitry to check external clock source

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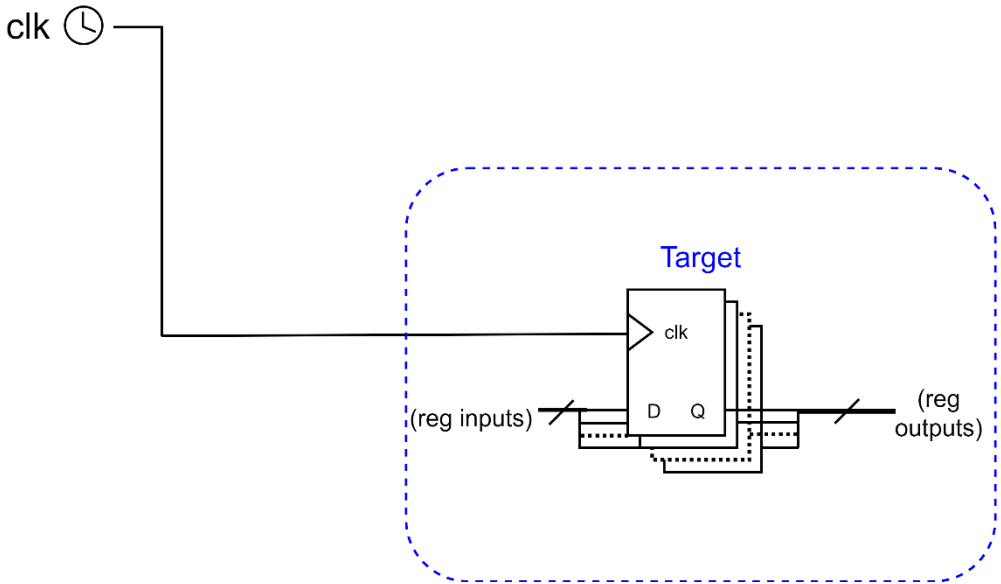

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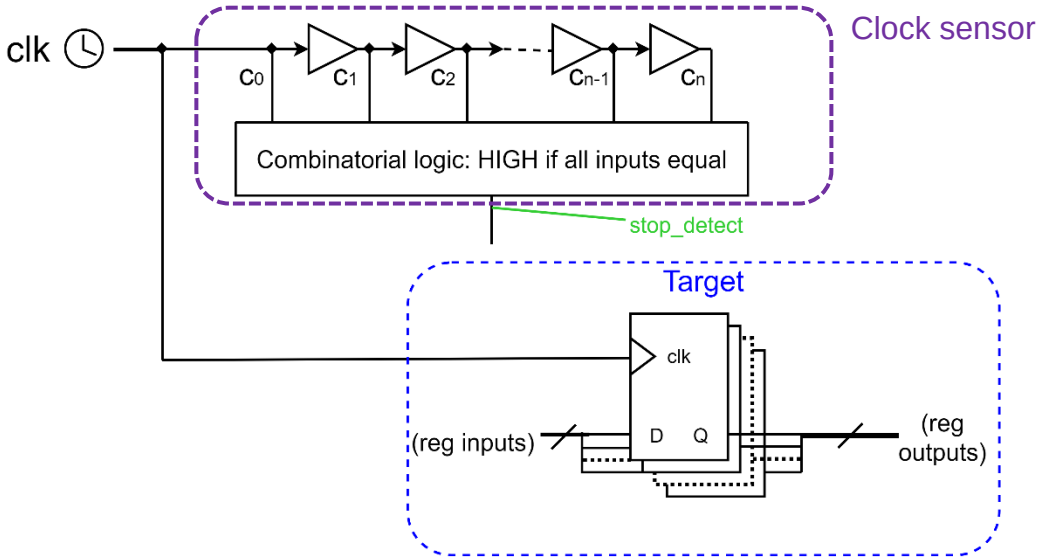

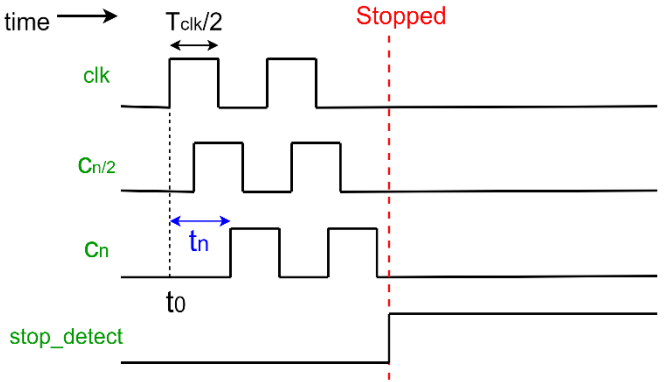

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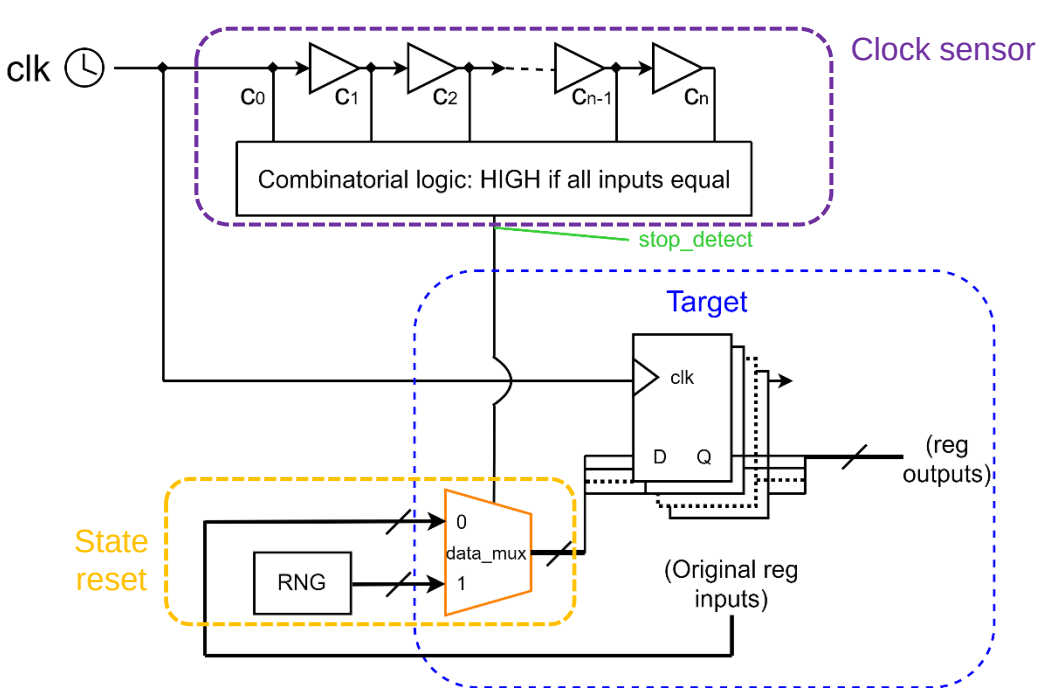

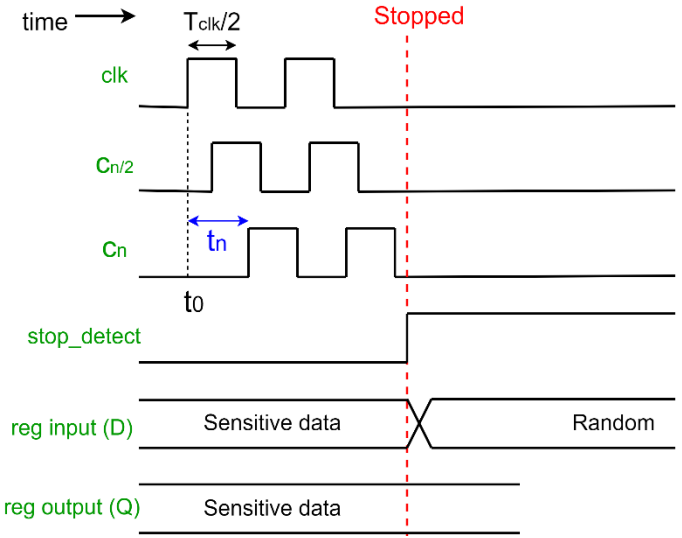

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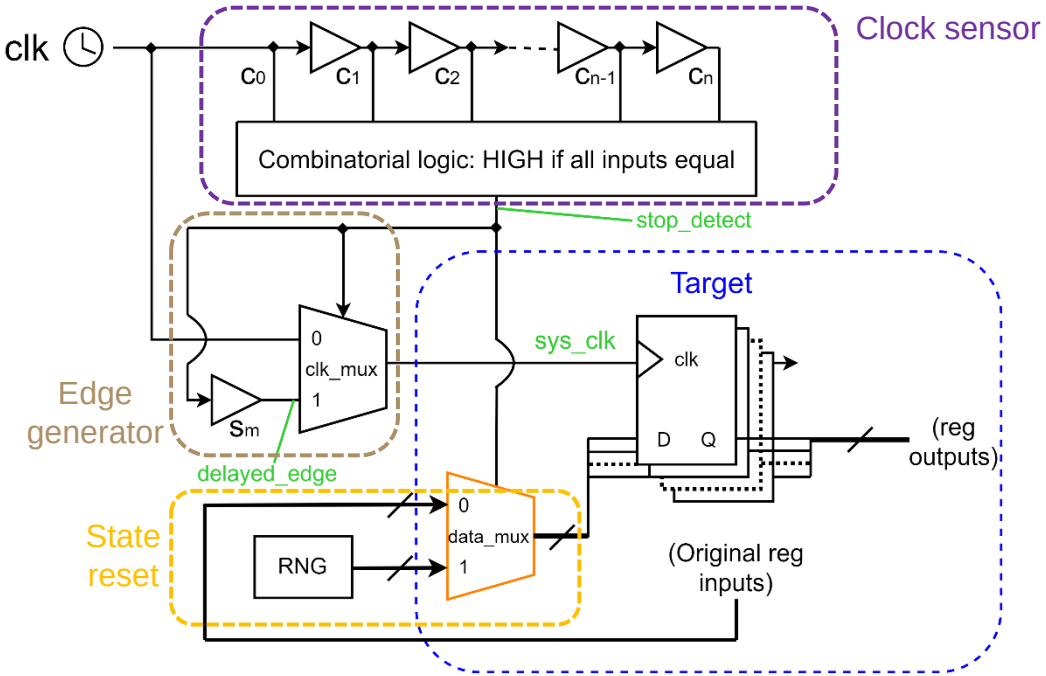

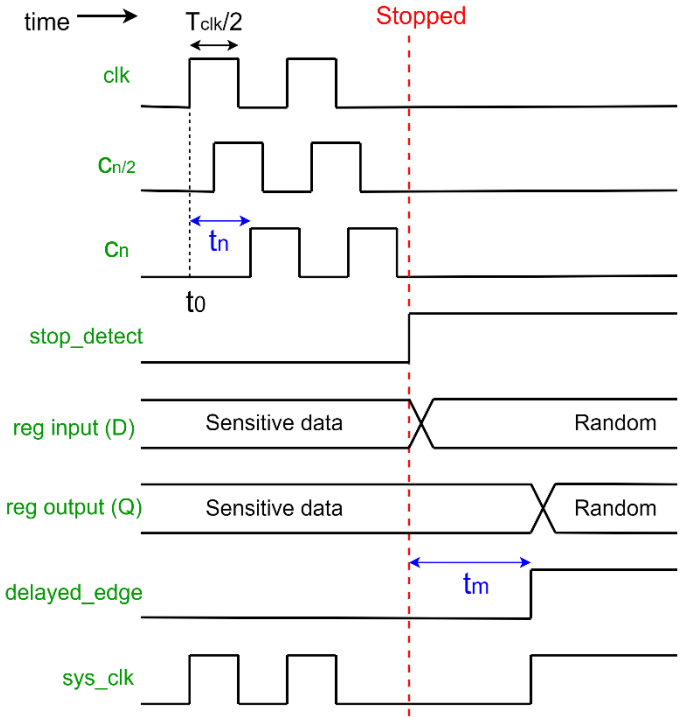

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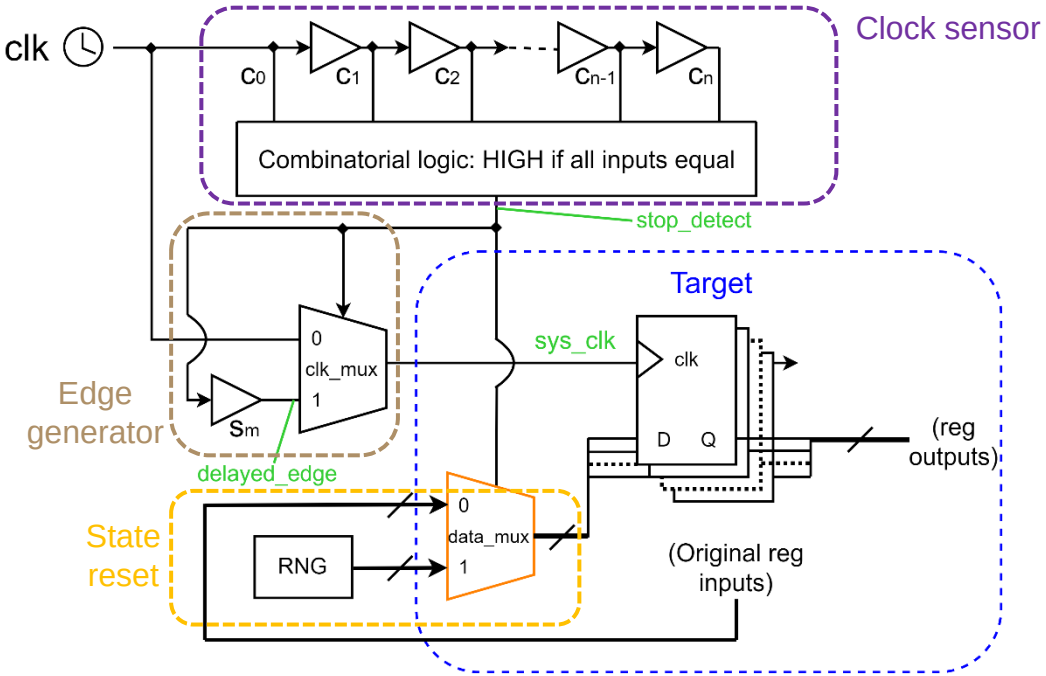
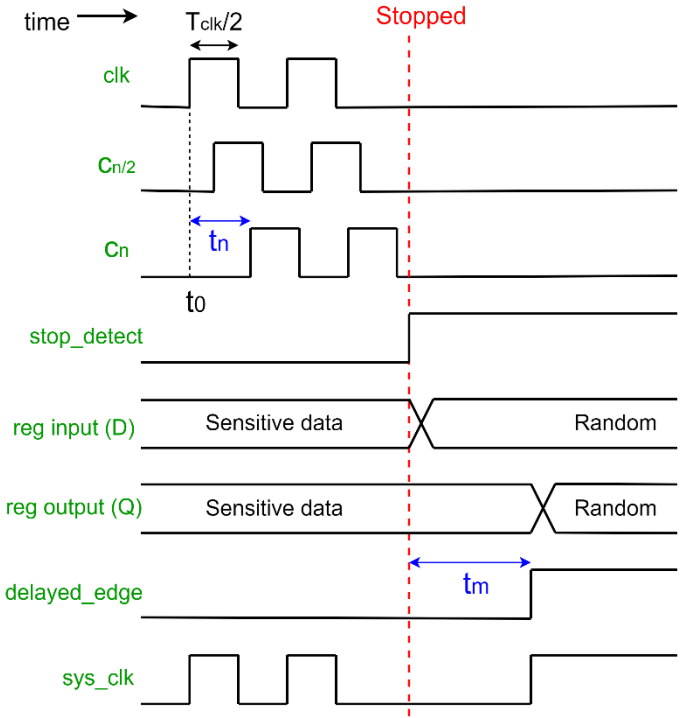
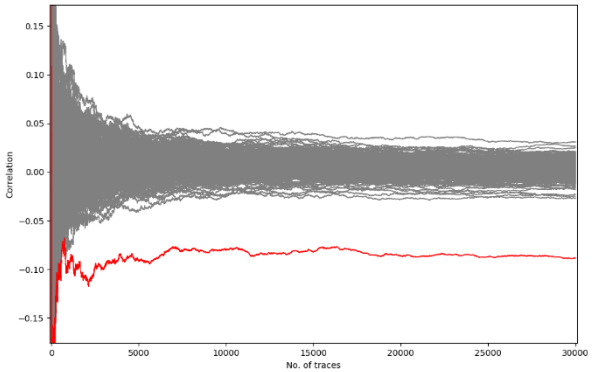




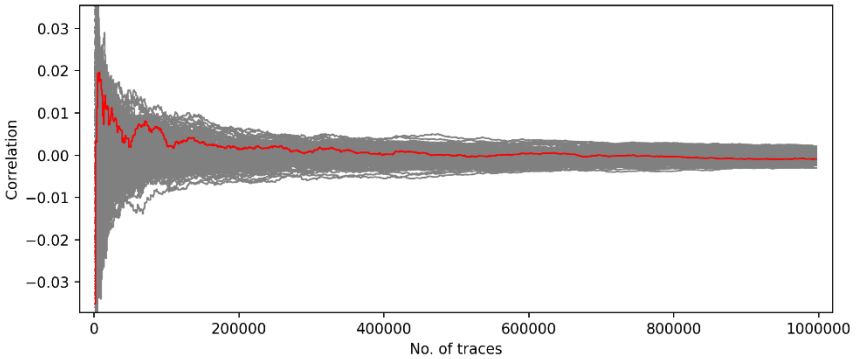
Assuming target operates in MHz range, BT can clear registers within **1µs** (<< 200µs)

Borrowed Time evaluation

Without countermeasure



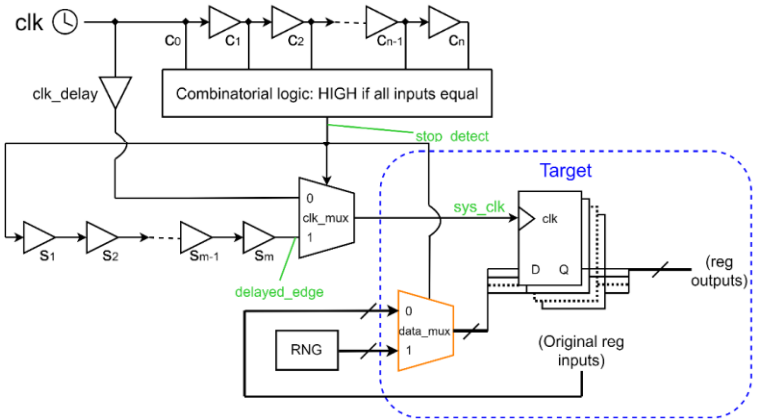
With Borrowed Time



Borrowed Time

- Flexible in-chip design to protect against static SCA
- Can allow for operation over a given frequency range
- Clock glitching resilient
- Enables safe operation inside clock-gated system
- Modest relative overhead

Paper



Code