GadgetMeter: Quantitatively and Accurately Gauging the Exploitability of Speculative Gadgets

Qi Ling, Yujun Liang, Yi Ren, Baris Kasikci, Shuwen Deng

Purdue University, University of Washington, Tsinghua University

Spectre Attacks

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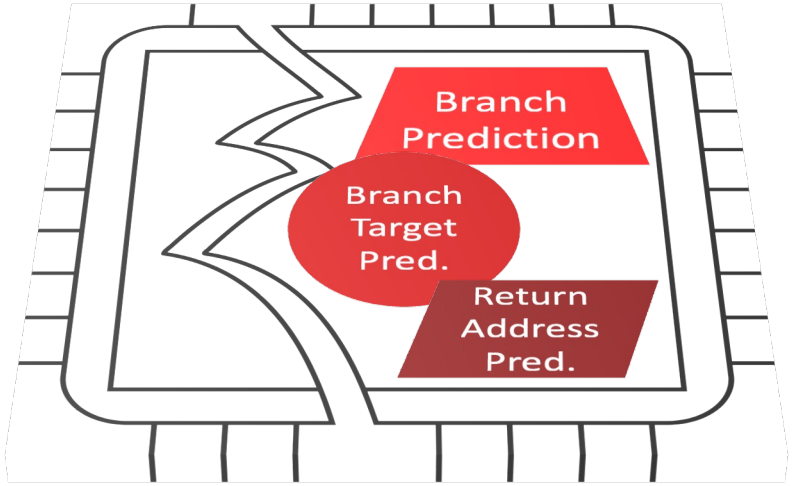

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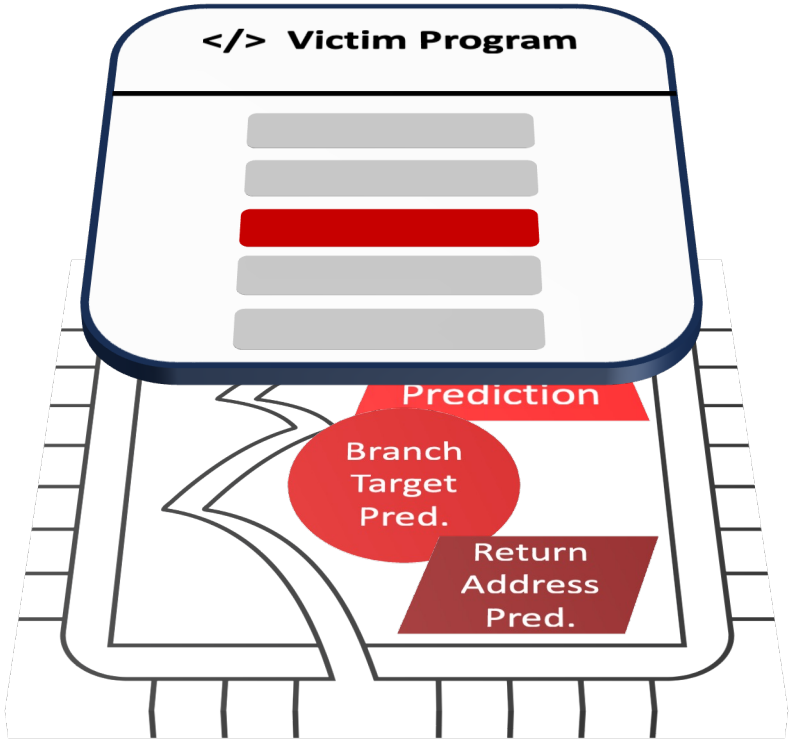

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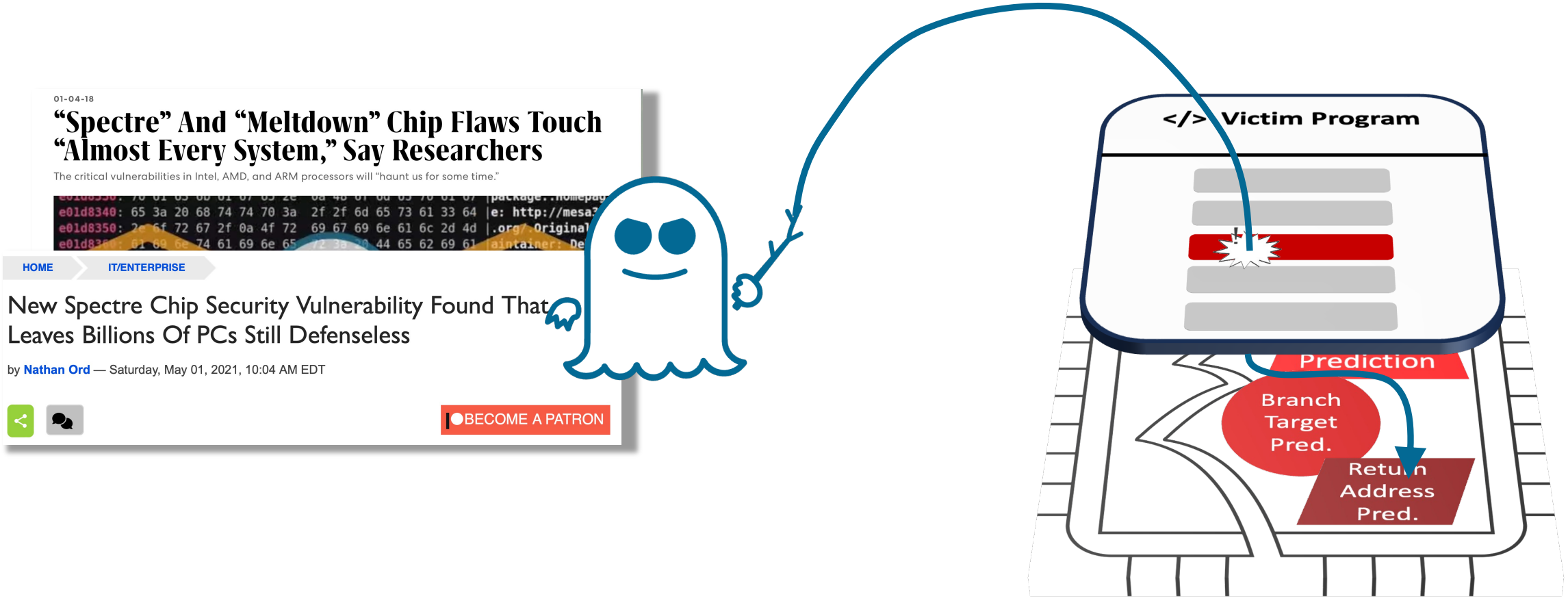

Spectre Attacks

01-04-18

“Spectre” And “Meltdown” Chip Flaws Touch “Almost Every System,” Say Researchers

The critical vulnerabilities in Intel, AMD, and ARM processors will “haunt us for some time.”

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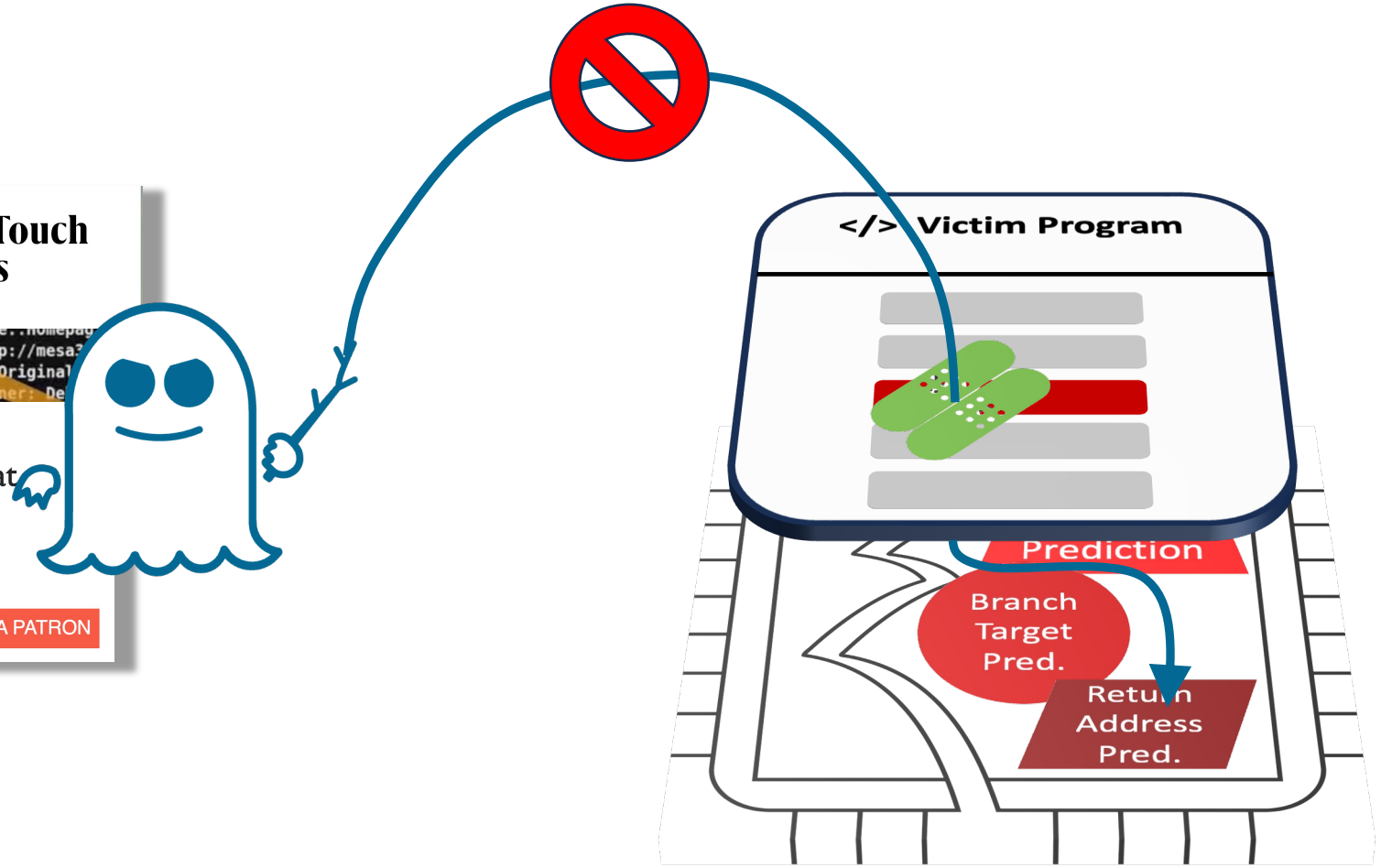
HOME IT/ENTERPRISE

New Spectre Chip Security Vulnerability Found That Leaves Billions Of PCs Still Defenseless

by Nathan Ord — Saturday, May 01, 2021, 10:04 AM EDT

BECOME A PATRON



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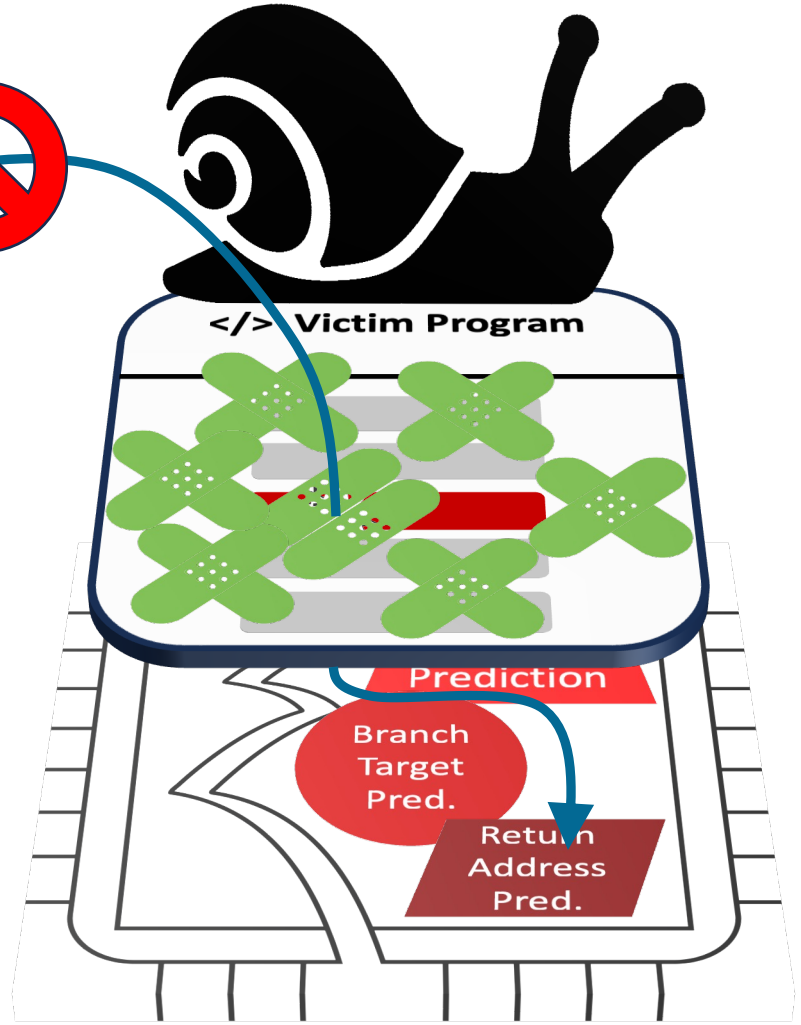

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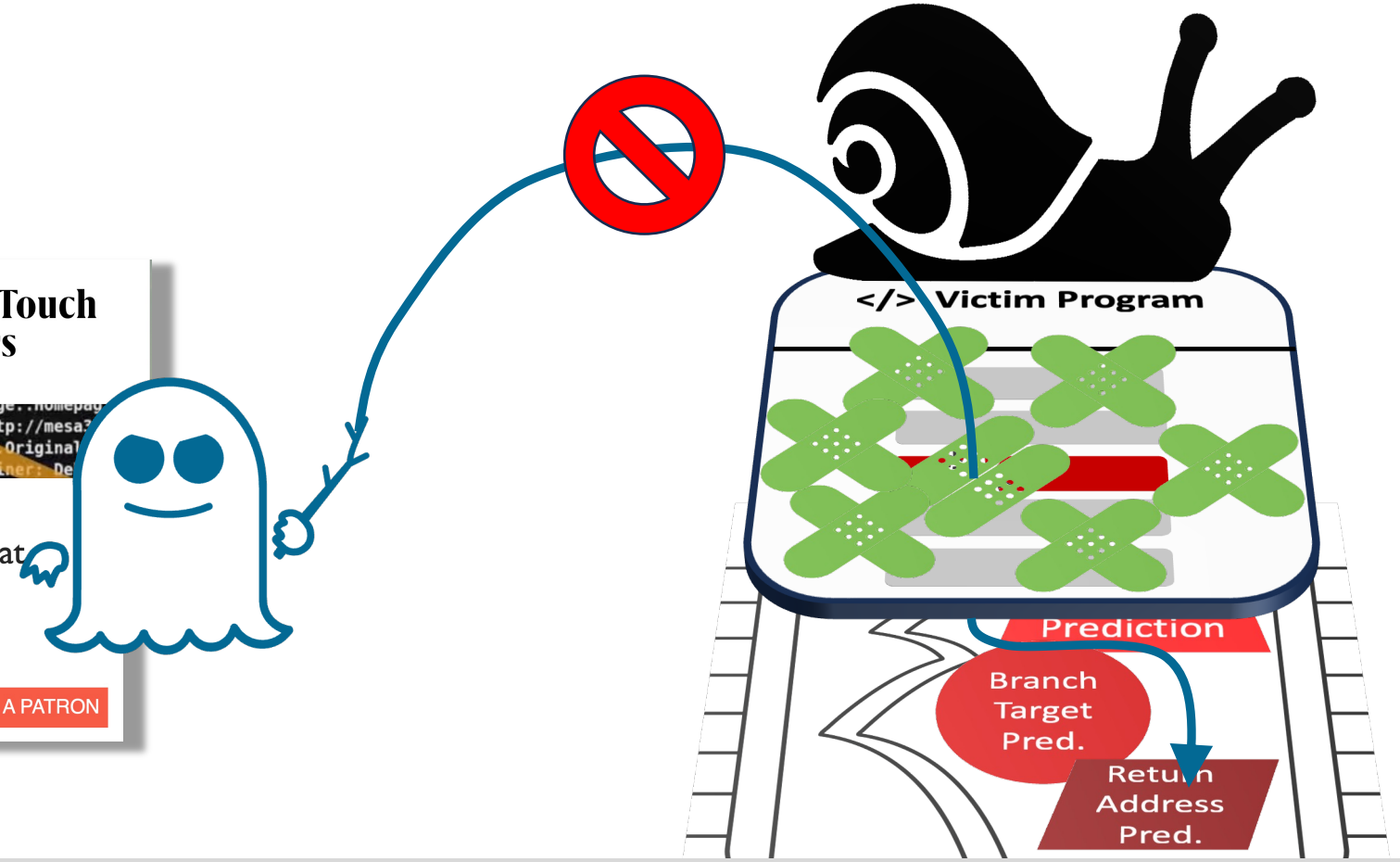

Accurate detection of Spectre gadgets.

What is a Spectre gadget?

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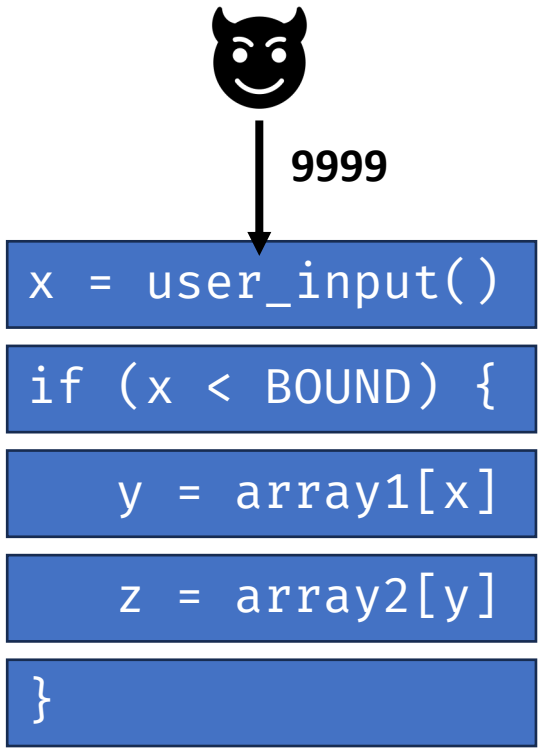

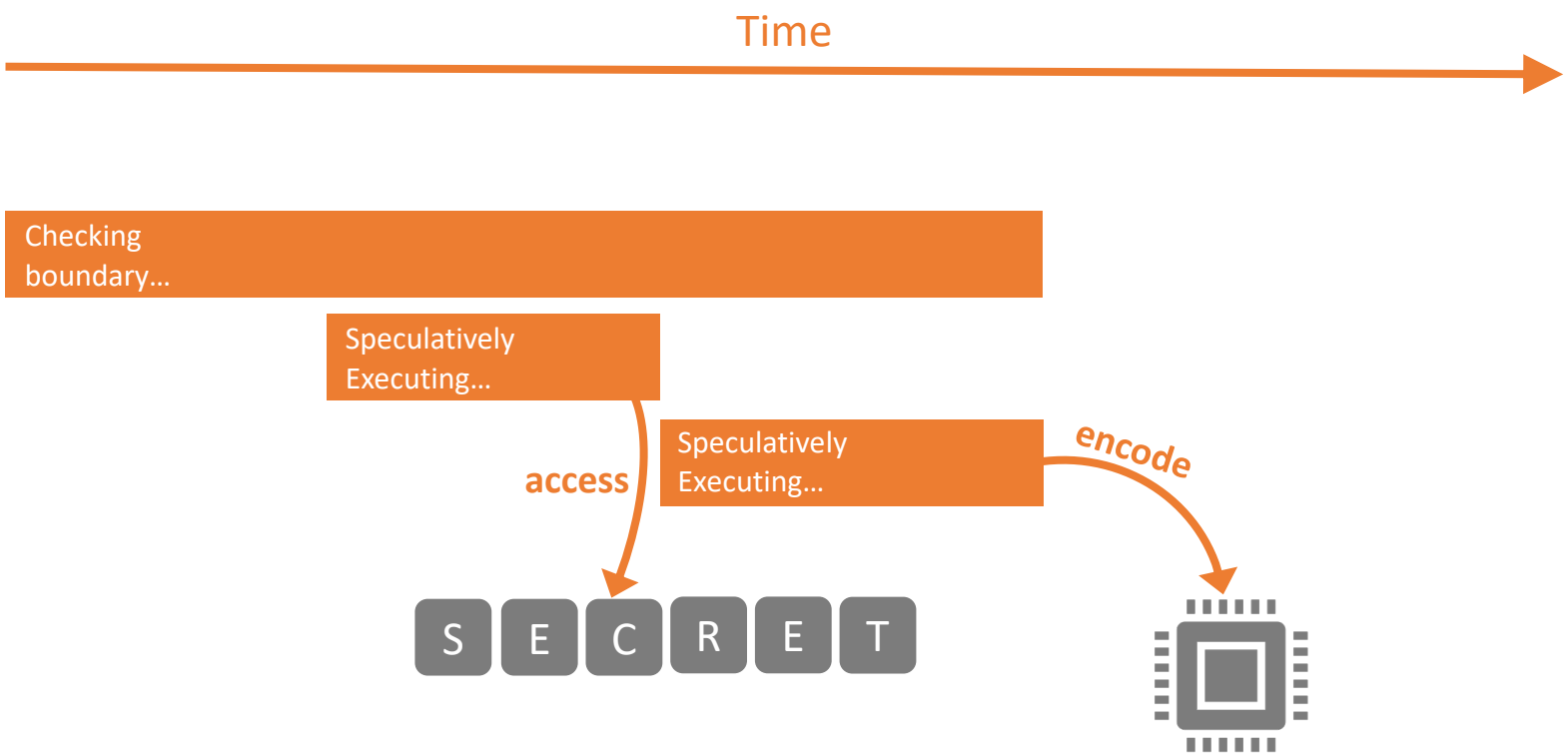

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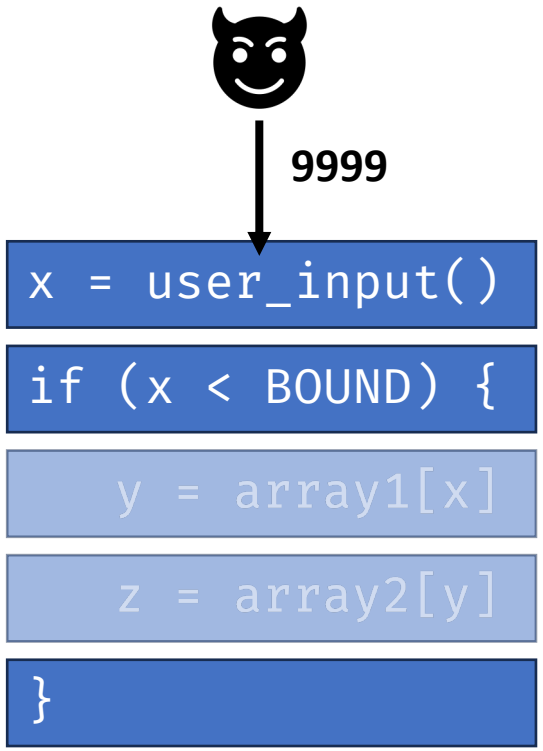

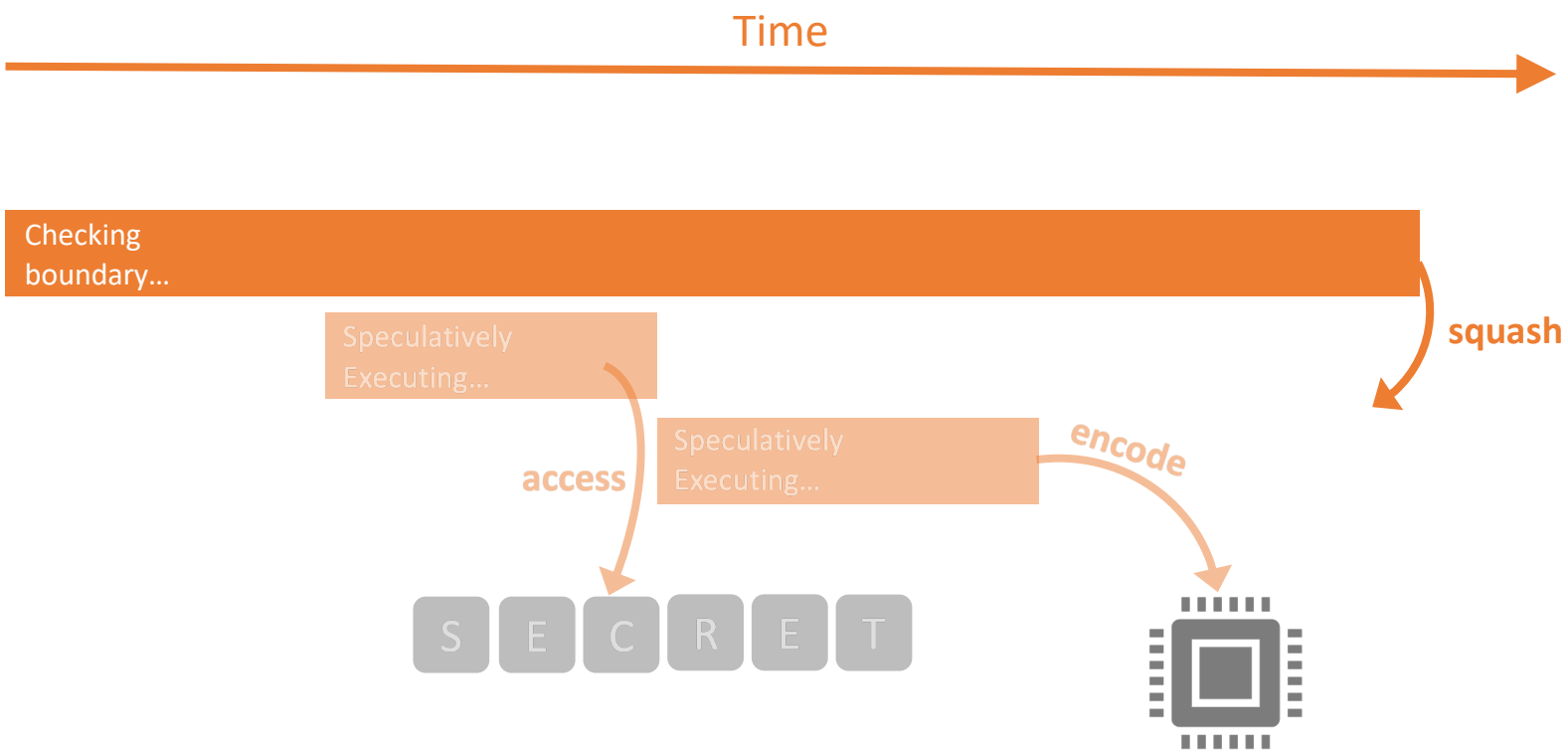

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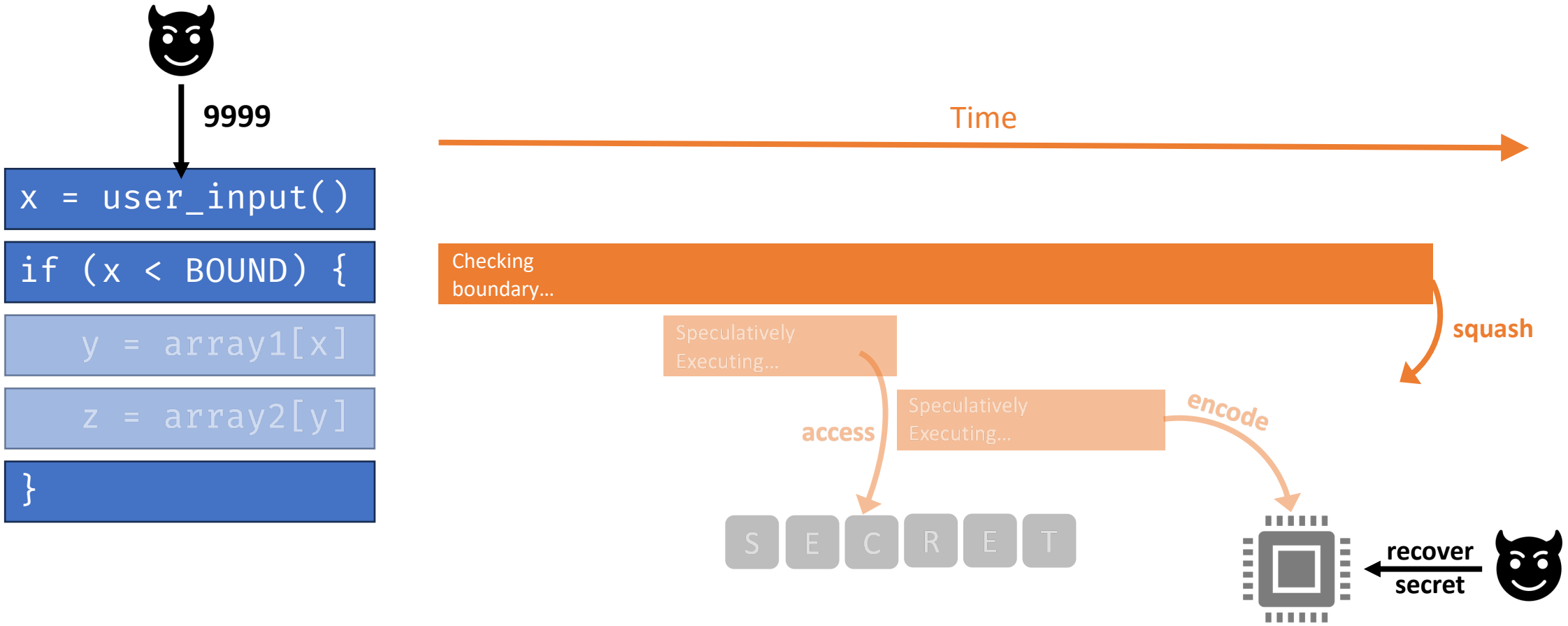

How do existing gadget scanners work?

```
x = user_input()

if (x < BOUND) {

    y = array1[x]

    z = array2[y]

}
```

How do existing gadget scanners work?

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x = user_input()

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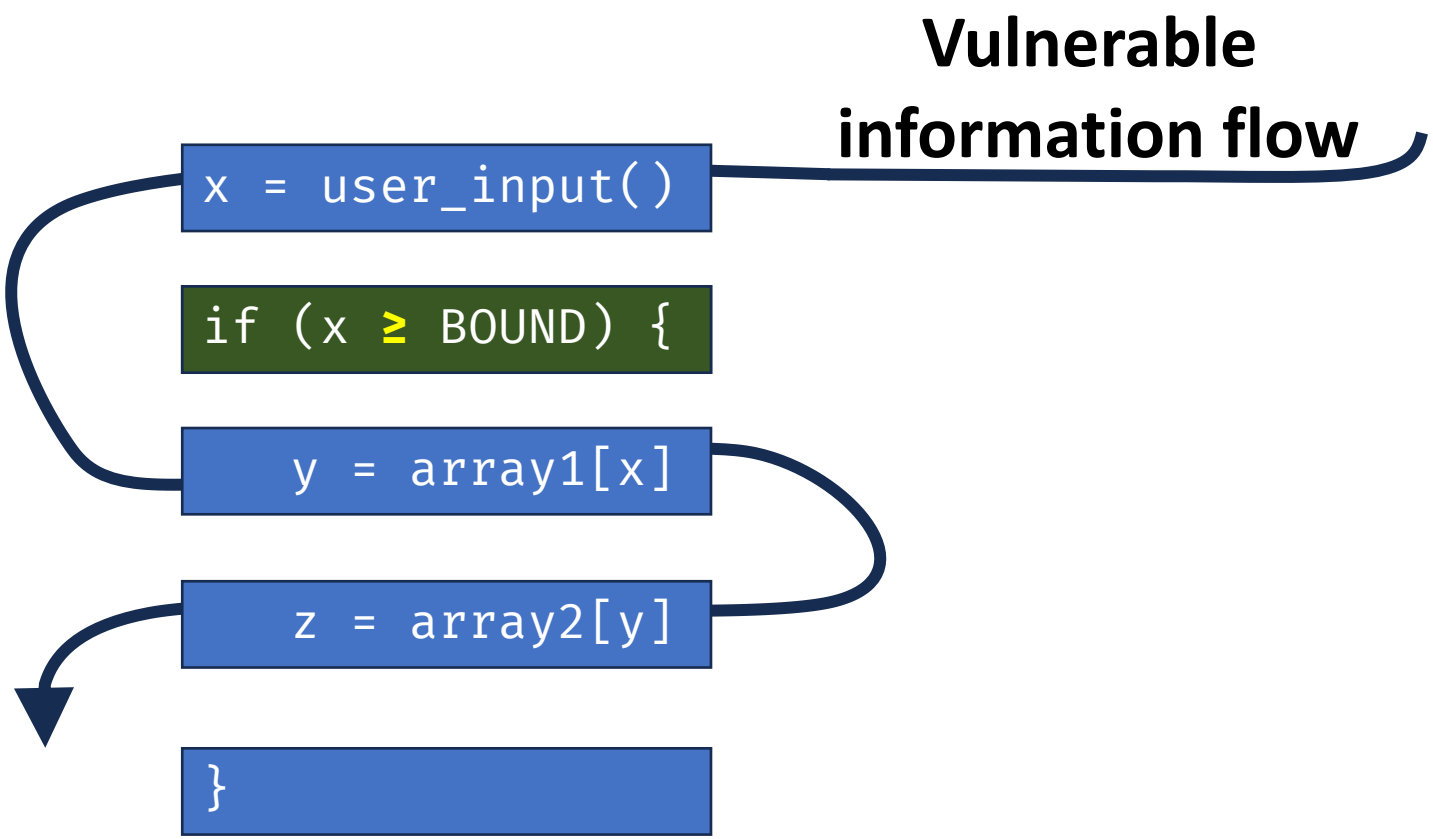

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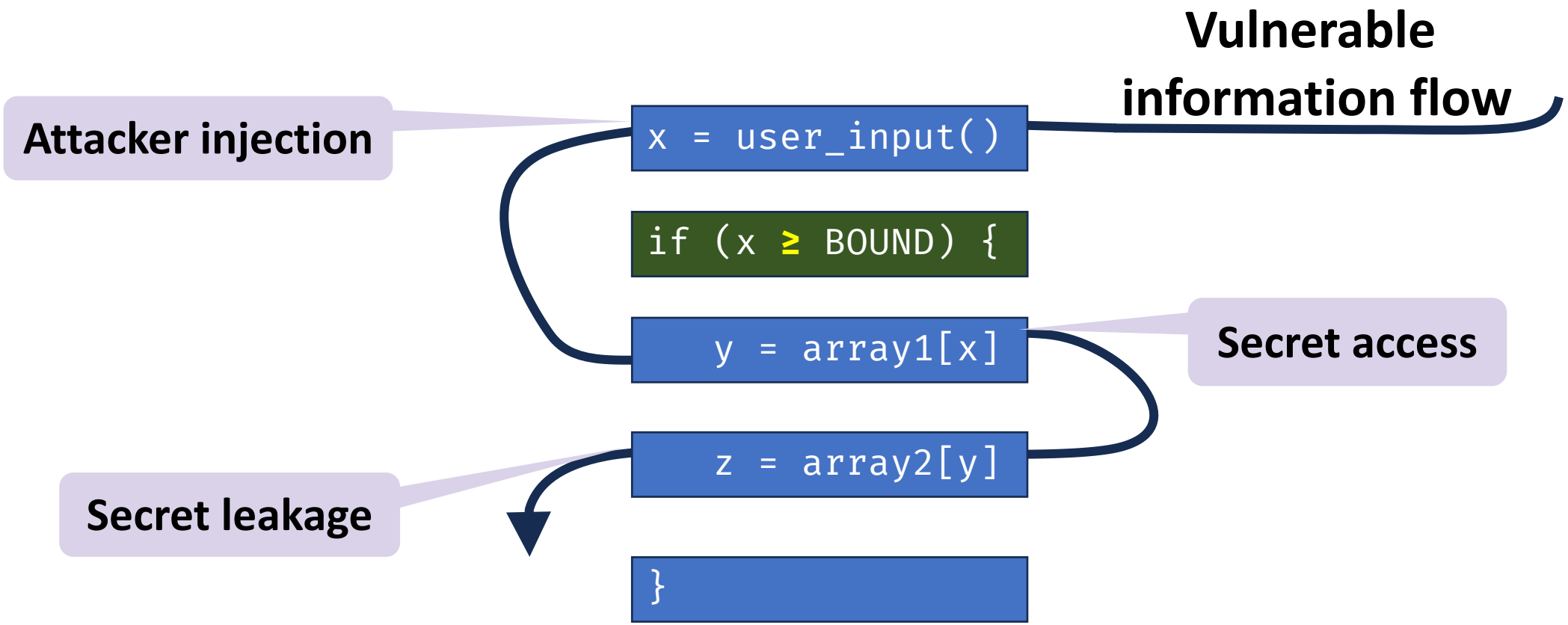
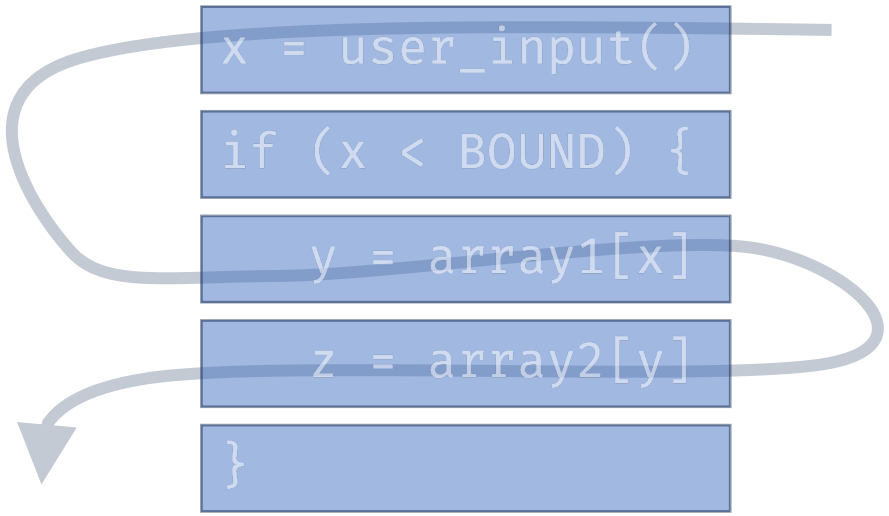


Missing piece: Timing condition



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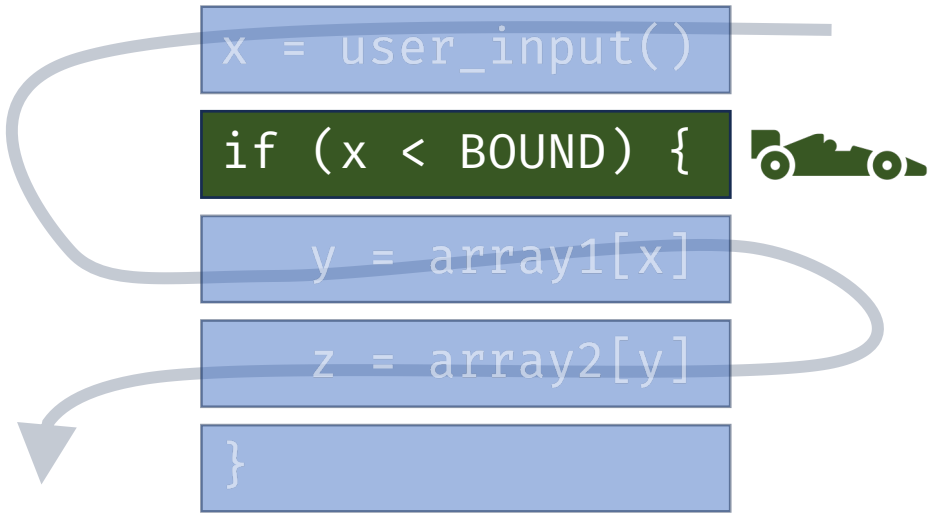

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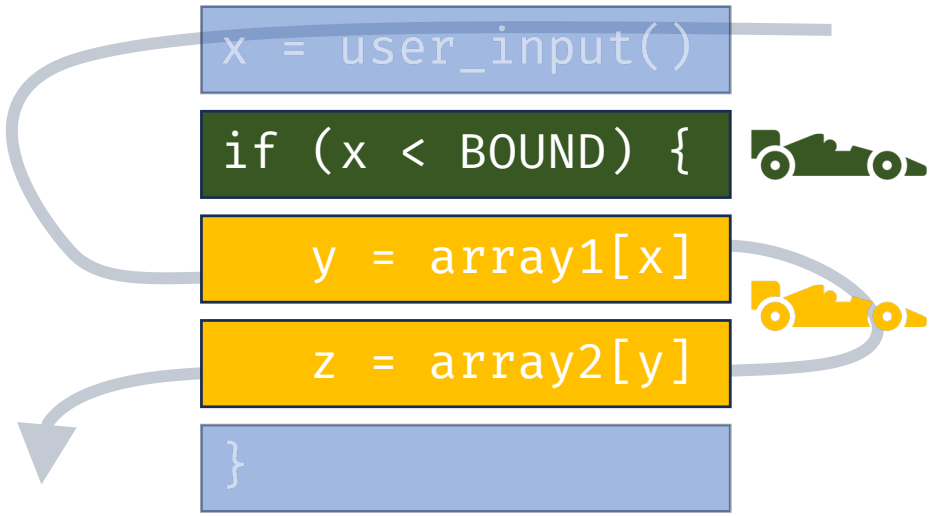

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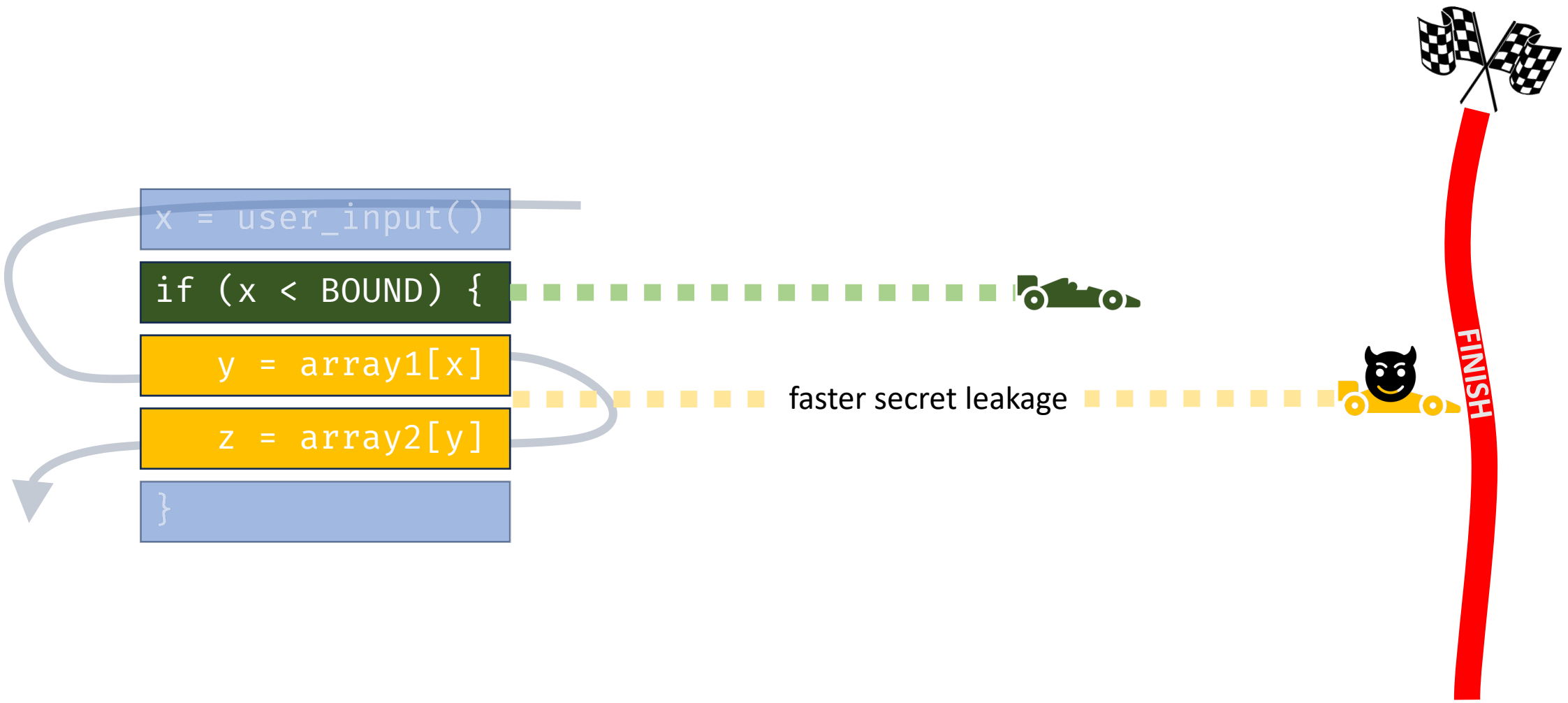

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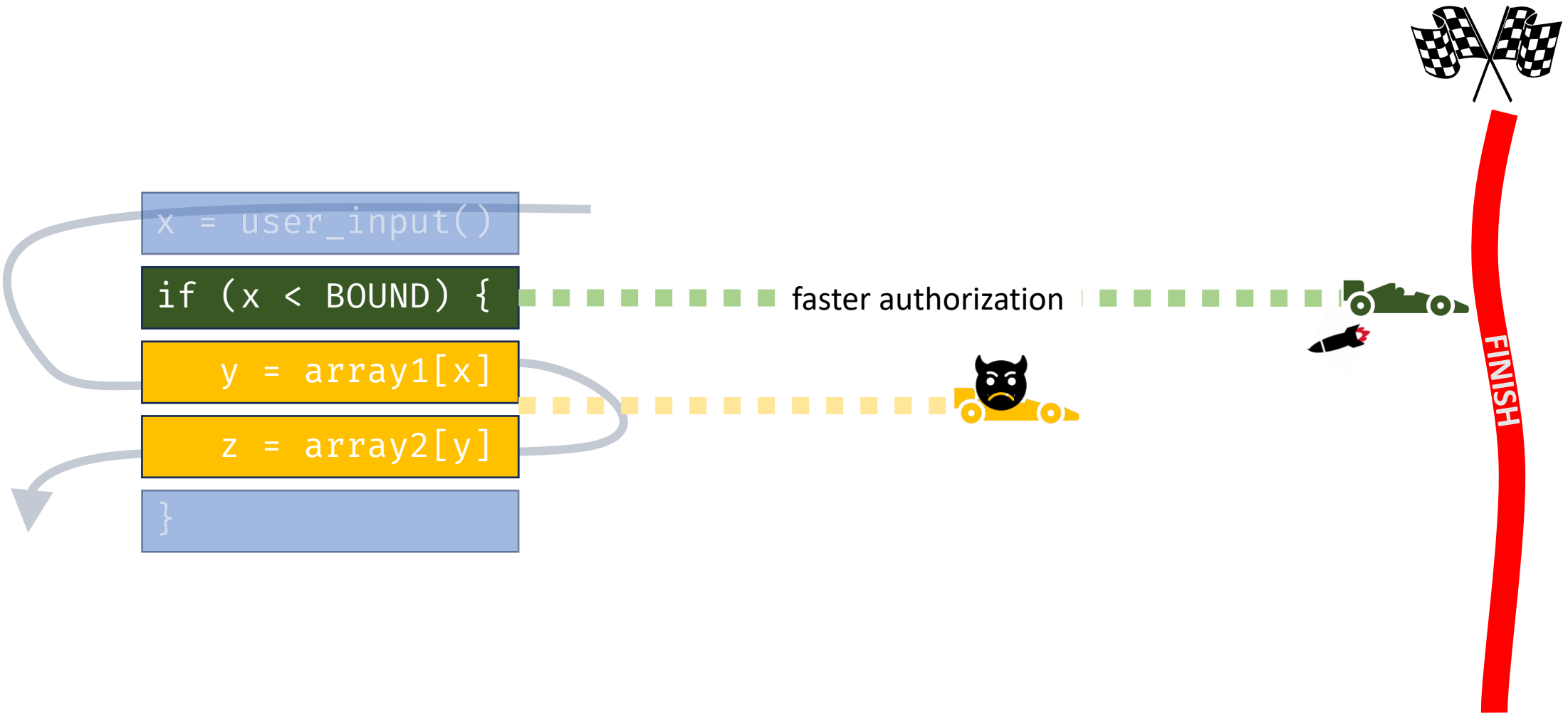

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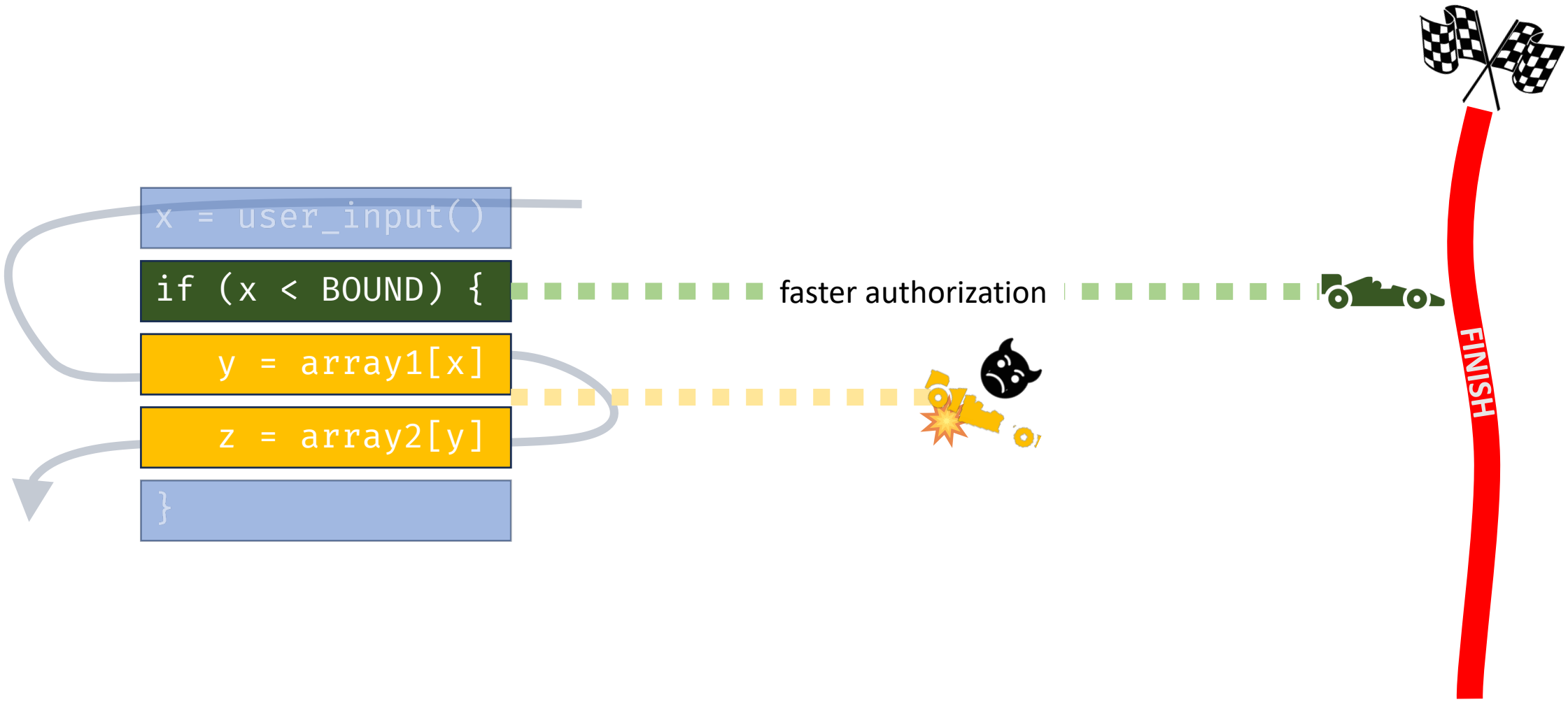

Satisfying the **timing condition** is necessary for a gadget to be **exploitable**.

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How do **existing works** model the timing condition?

Most scanners: Approximating with RoB size

```
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    y = array1[x]
    z = array2[y]
}
```
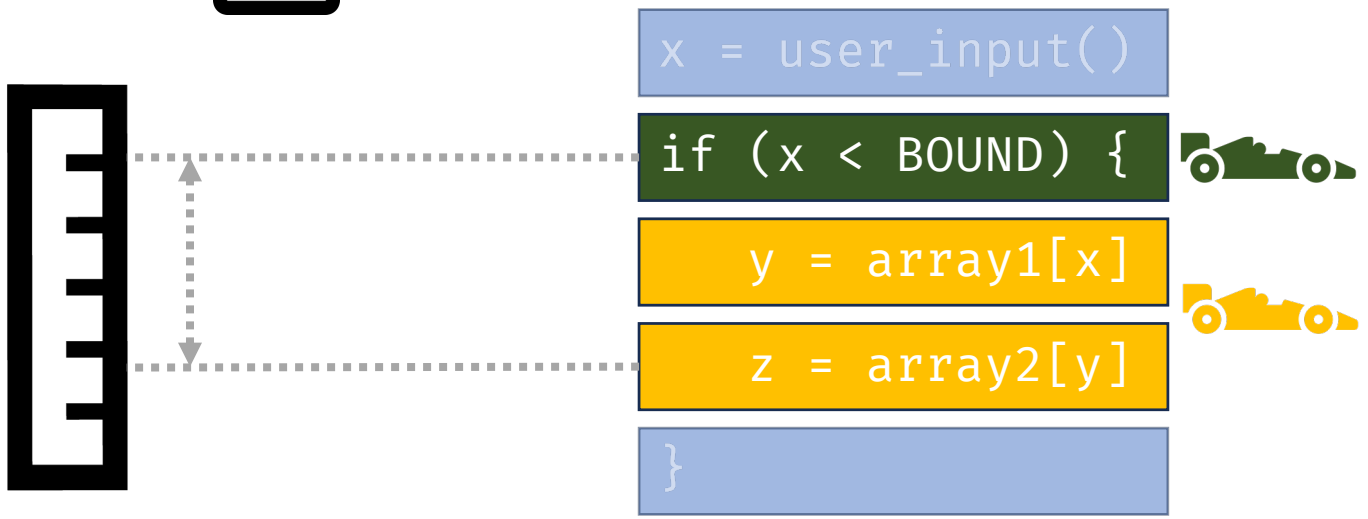
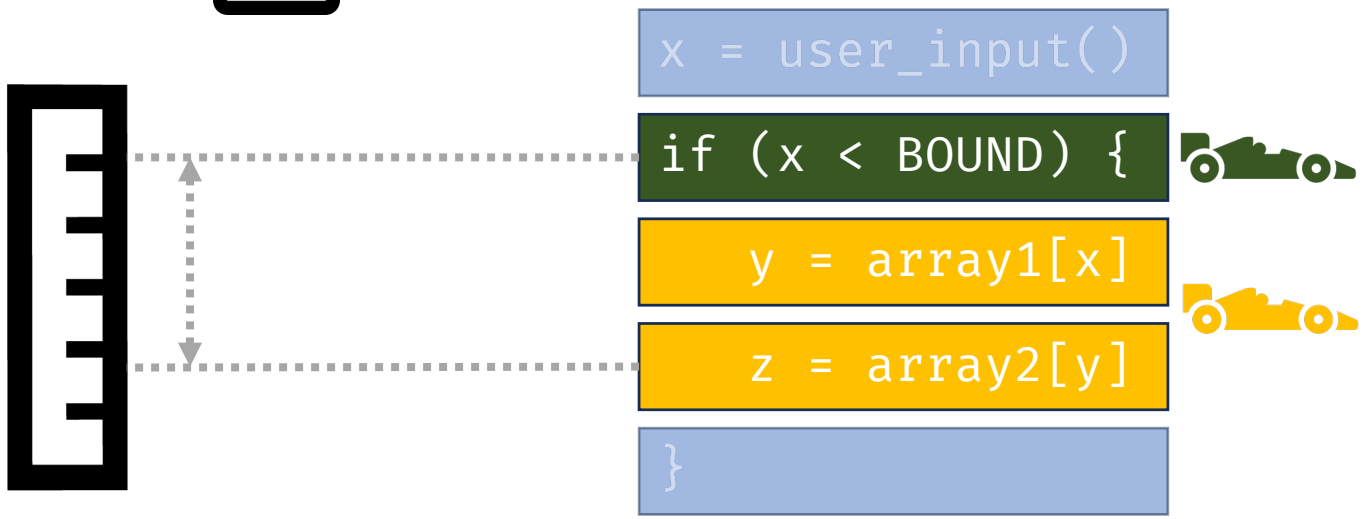

Most scanners: Approximating with RoB size

Fit in RoB ?



Most scanners: Approximating with RoB size

Fit in RoB ☑



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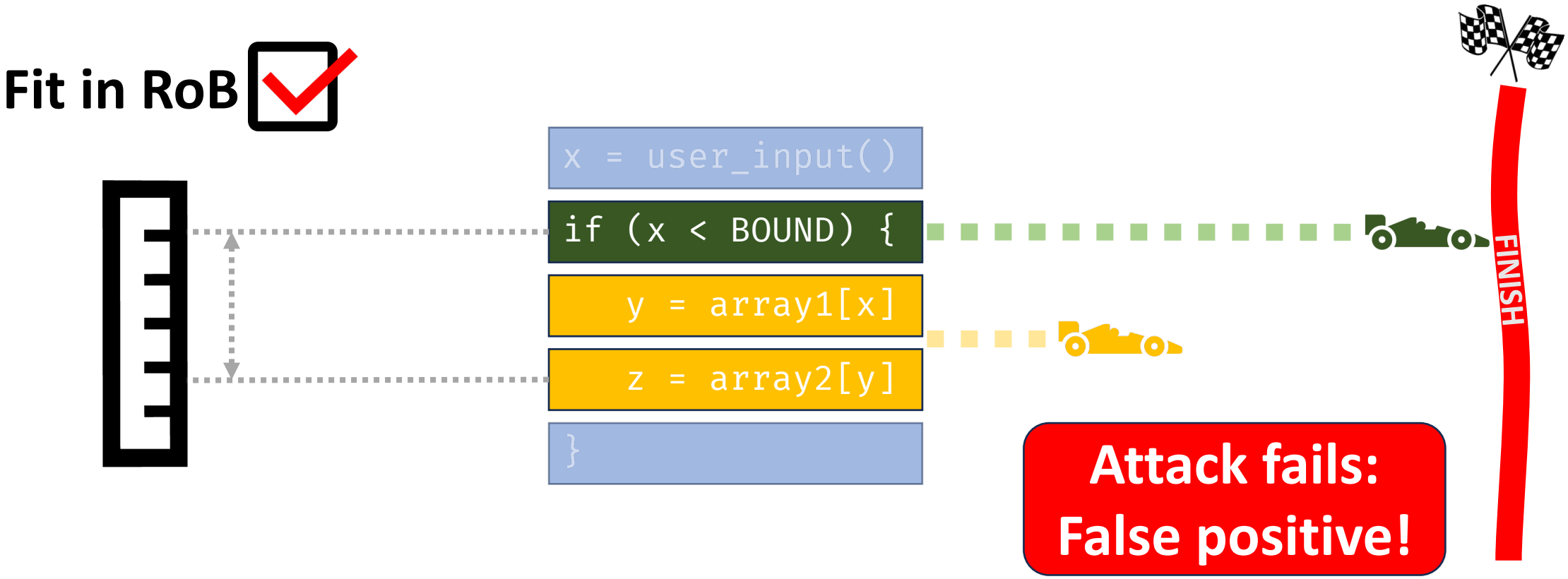
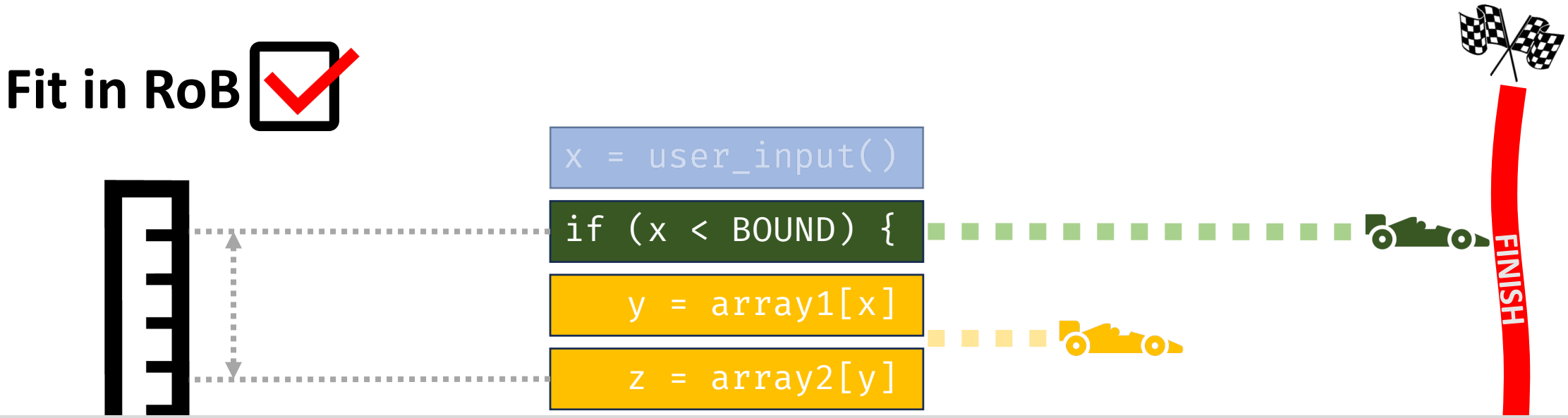
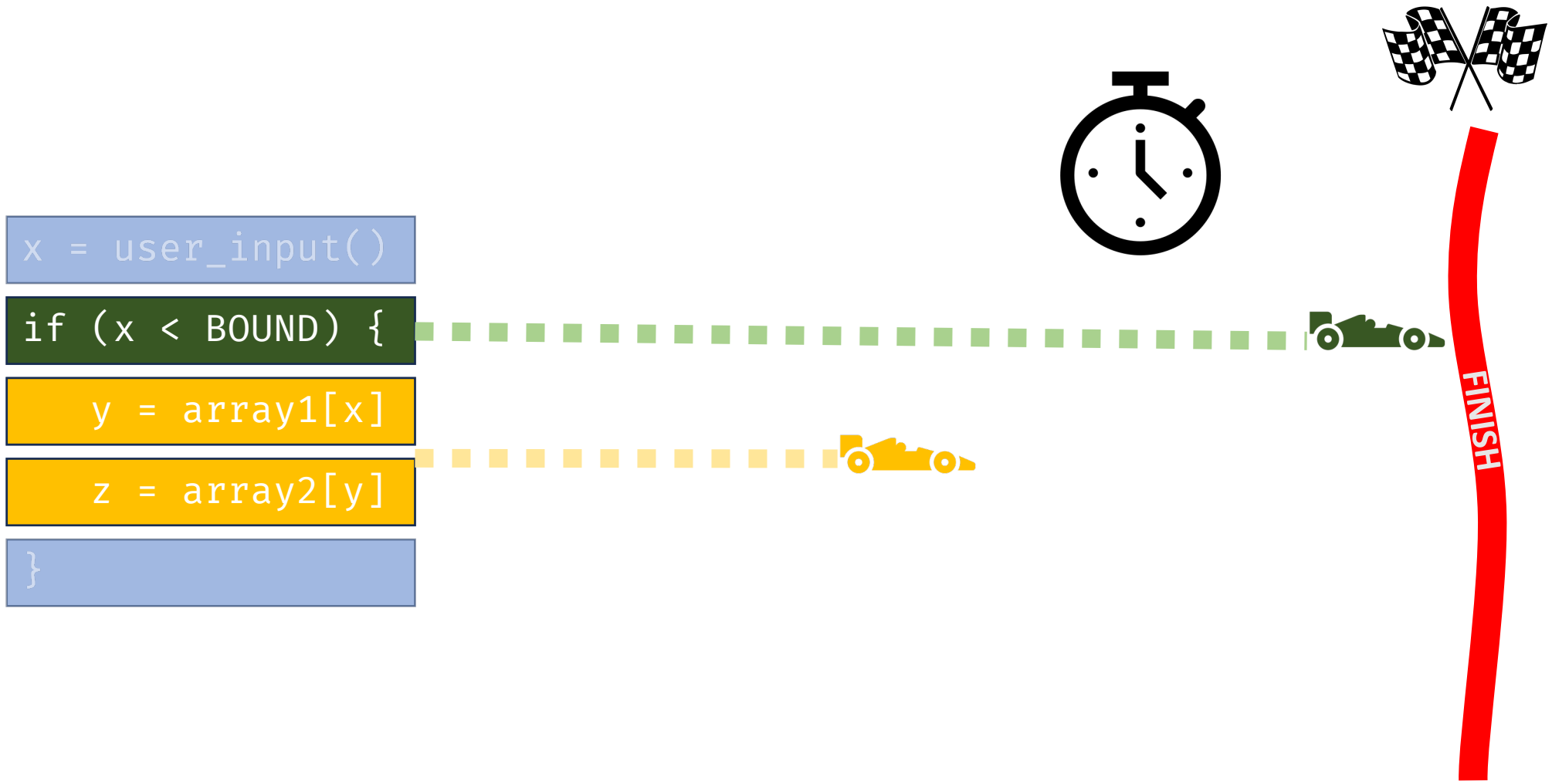


Most scanners: Approximating with RoB size



Measure the timing condition accurately!

Some others: Timing modelling



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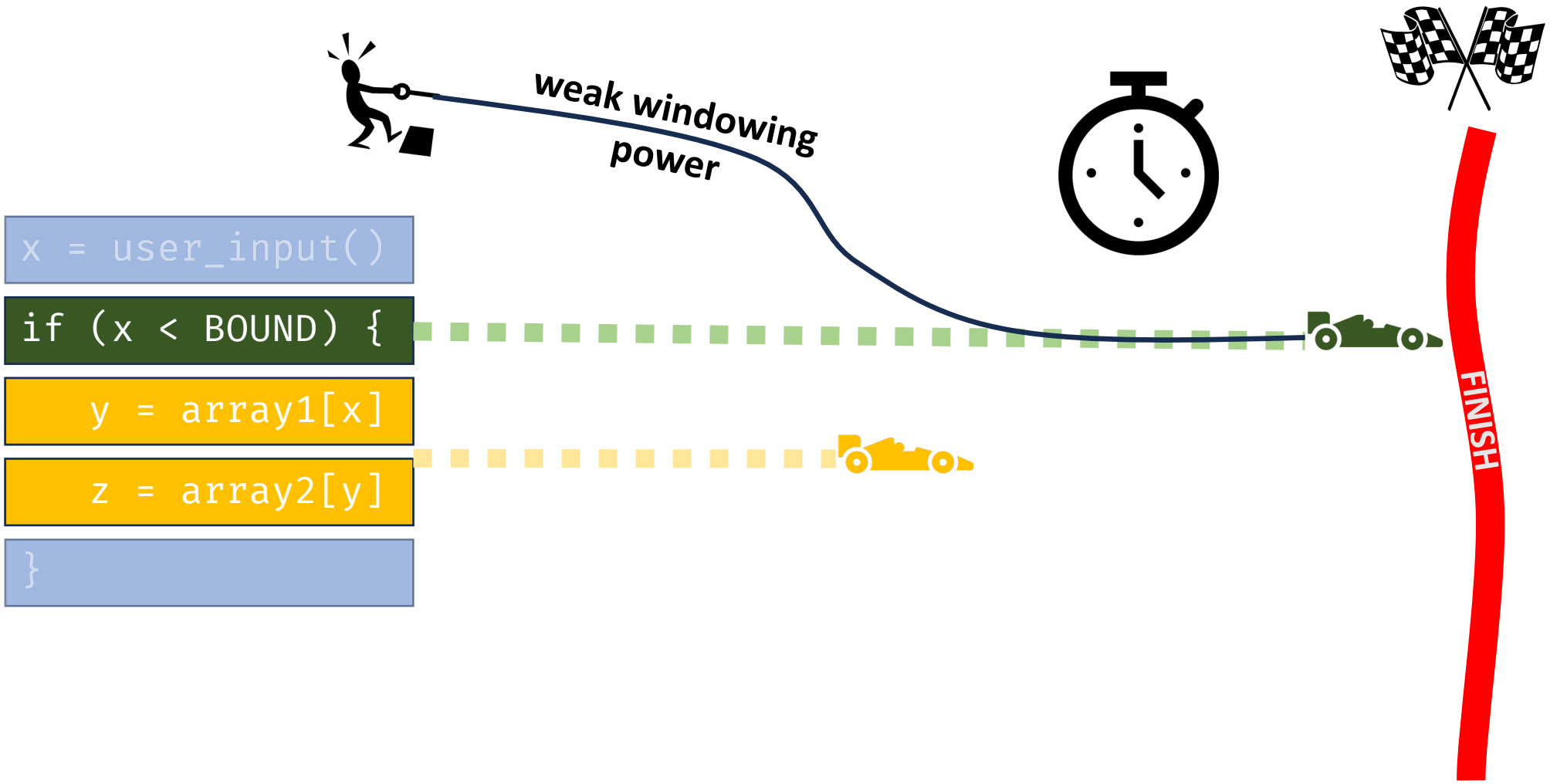

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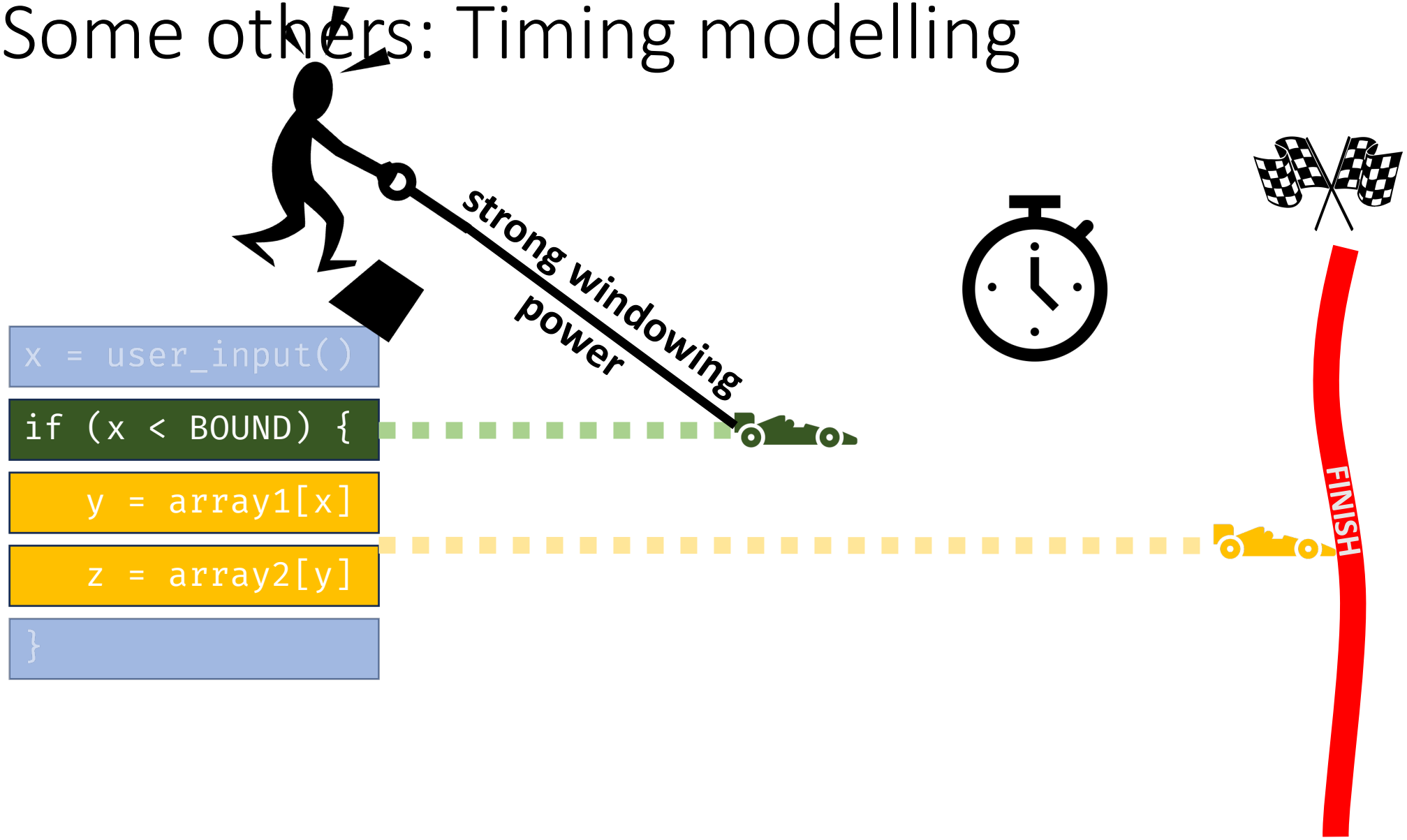

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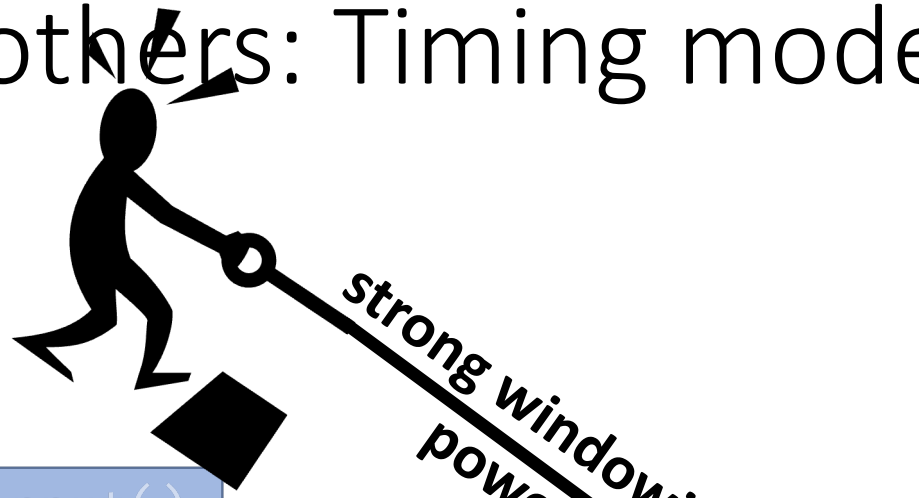

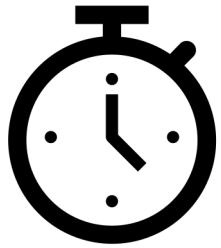


```
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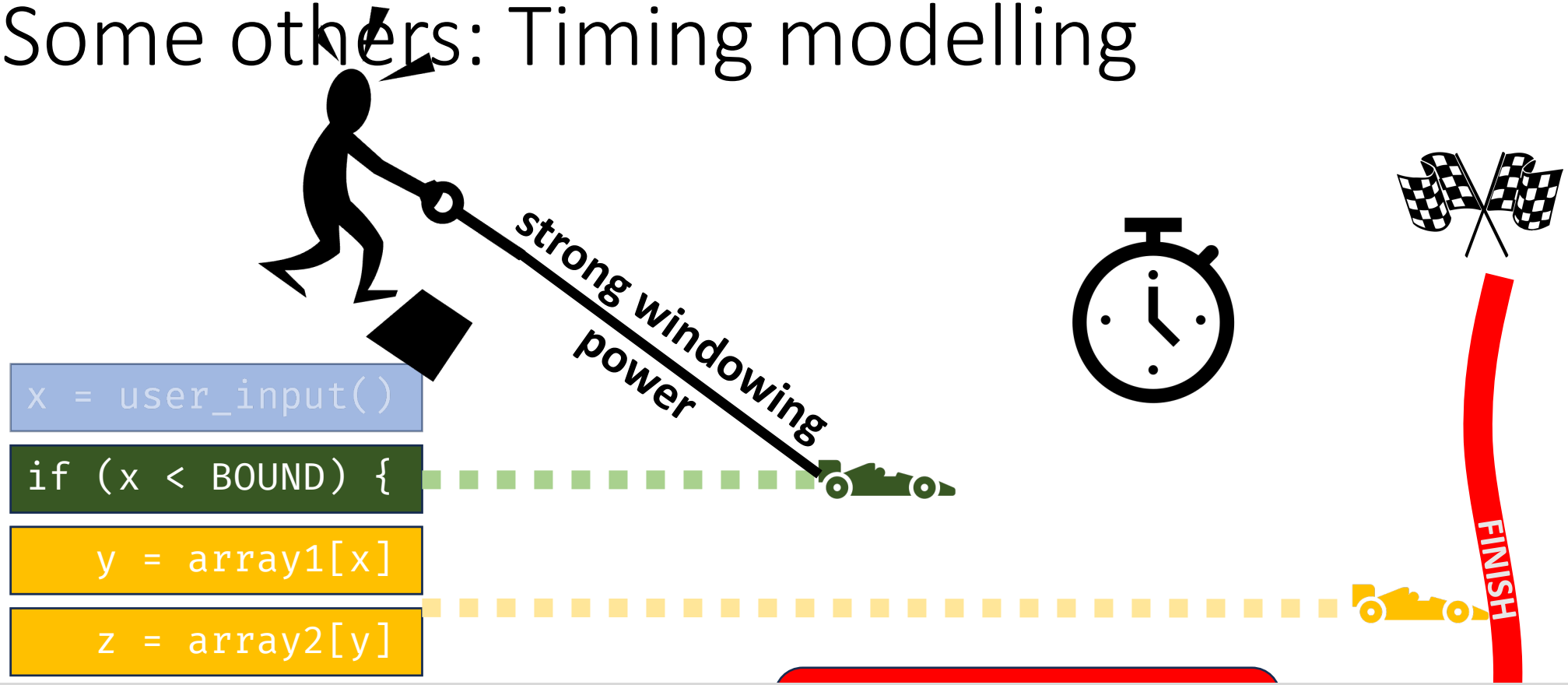
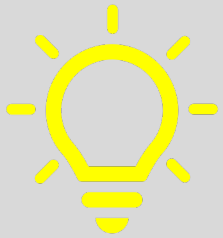
Attack succeeds:
False negative!

Some others: Timing modelling

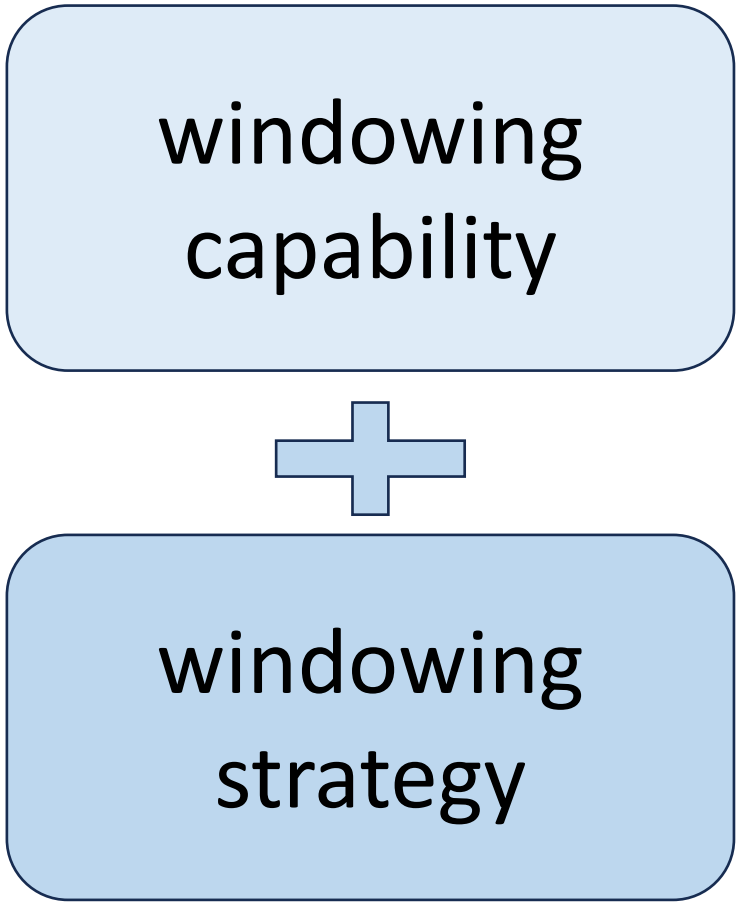




Measure the timing condition accurately,

under strong windowing power!

Our approach: Modelling windowing power

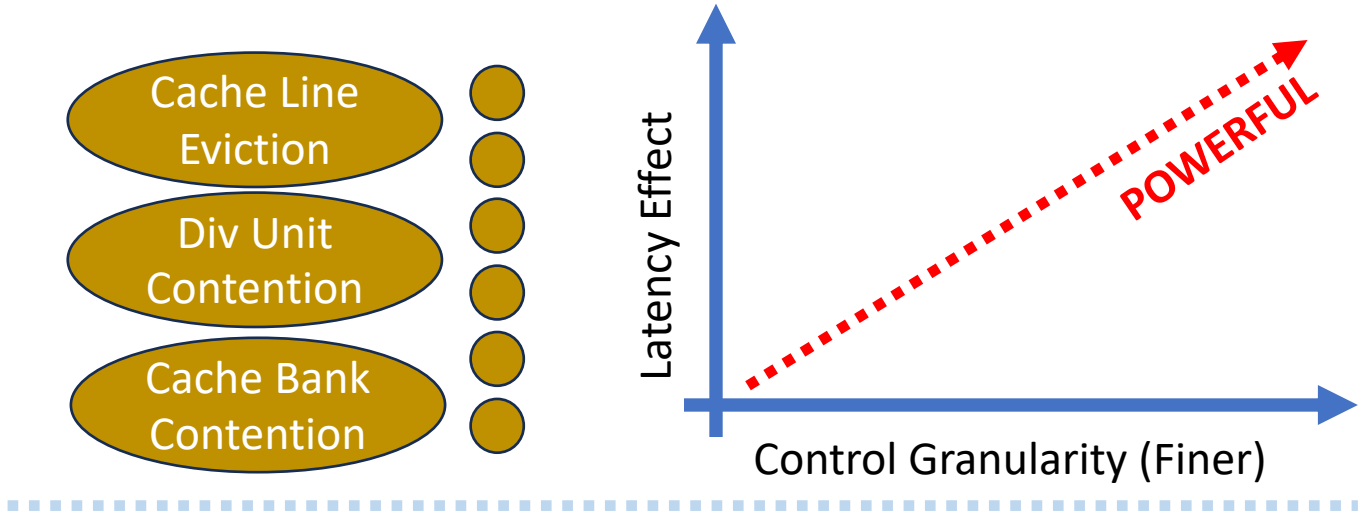


Our approach: Modelling windowing power

windowing capability

+

windowing strategy



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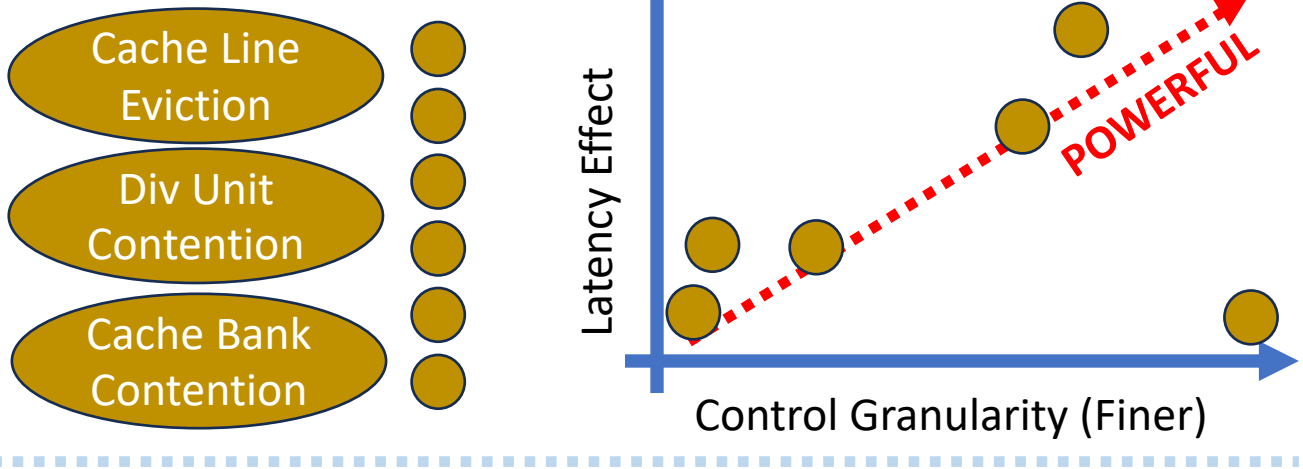

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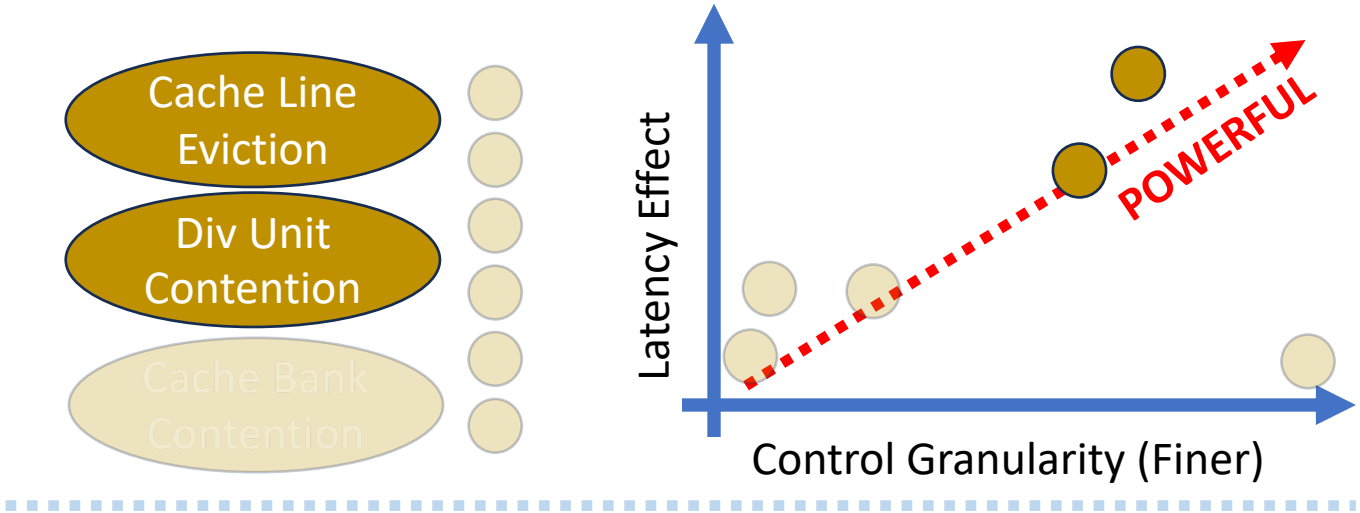


Our approach: Modelling windowing power

windowing capability

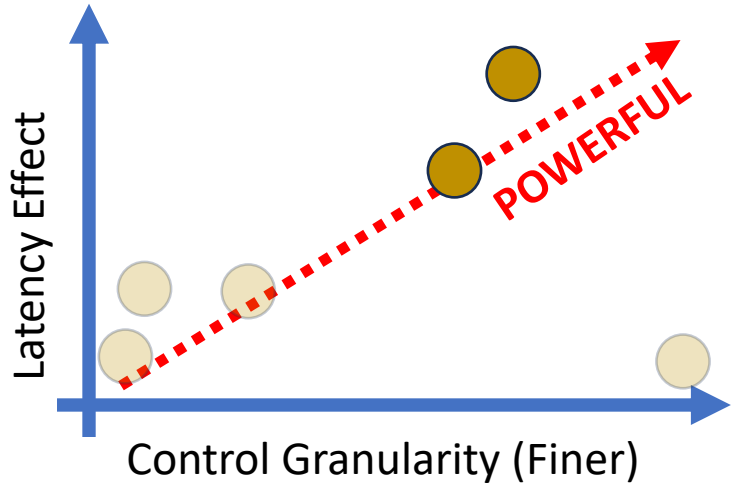
+

windowing strategy

Cache Line Eviction

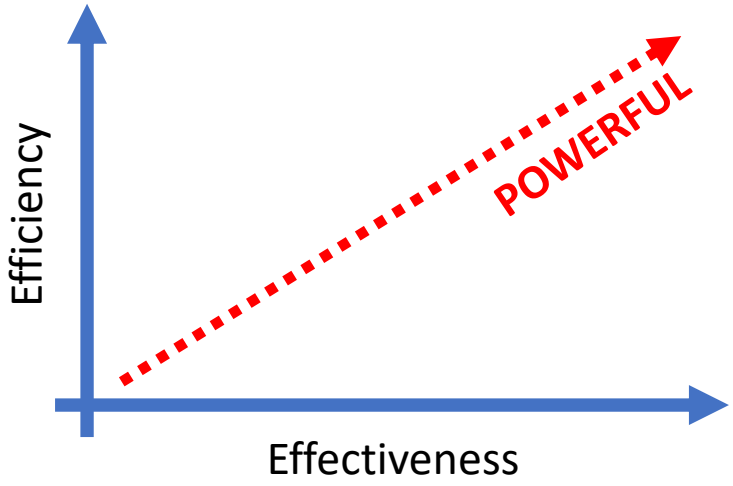
Div Unit Contention

Cache Bank Contention



Naïve Strategy

Brute force Strategy



Our approach: Modelling windowing power

windowing capability

+

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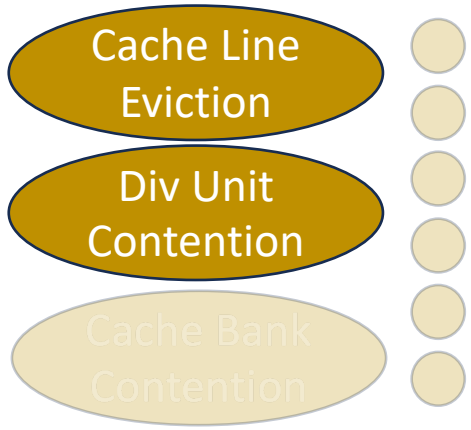

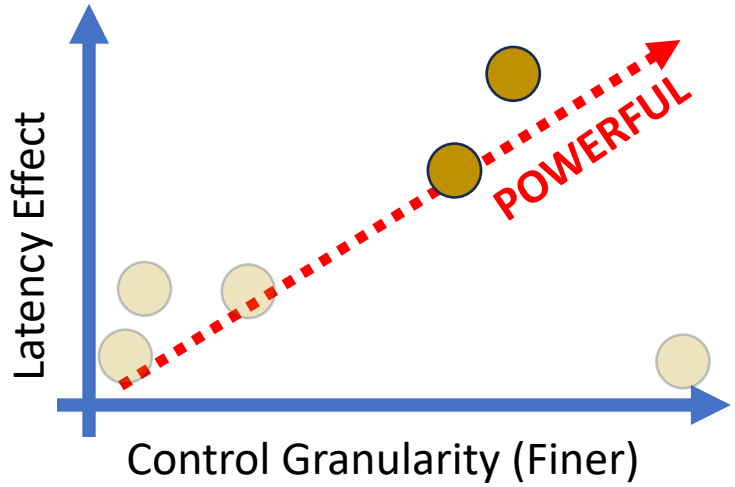

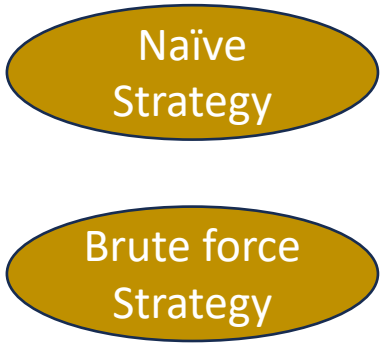

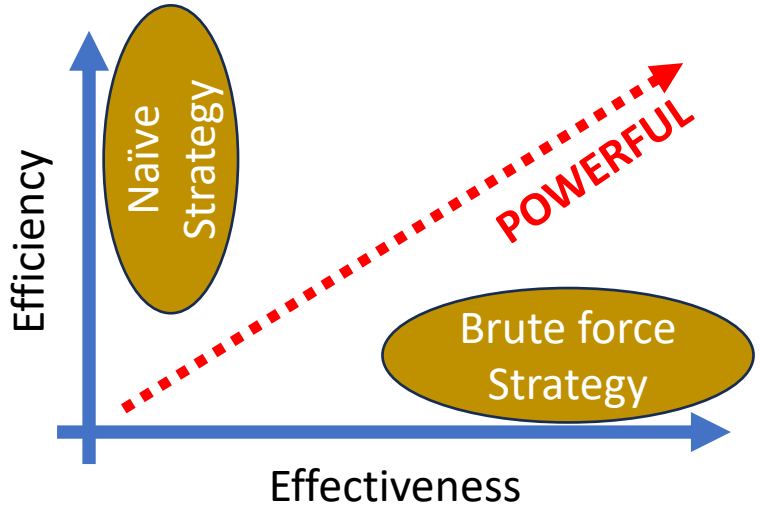

Our approach: Modelling windowing power

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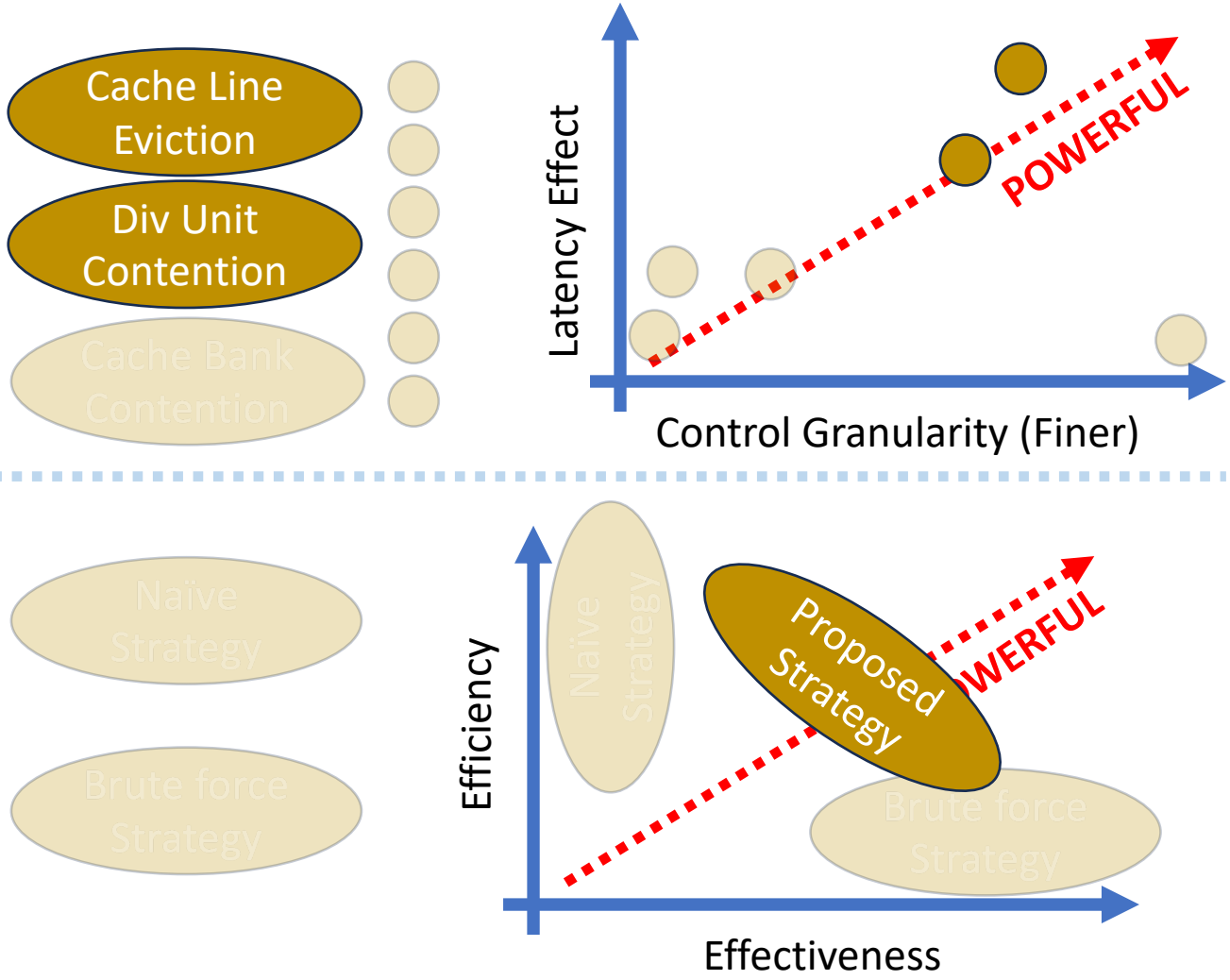

Well, how do we evaluate gadgets?

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Step A: **Modelling** timing condition

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Step A: **Modelling** timing condition

Step B: **Simulating** windowing power

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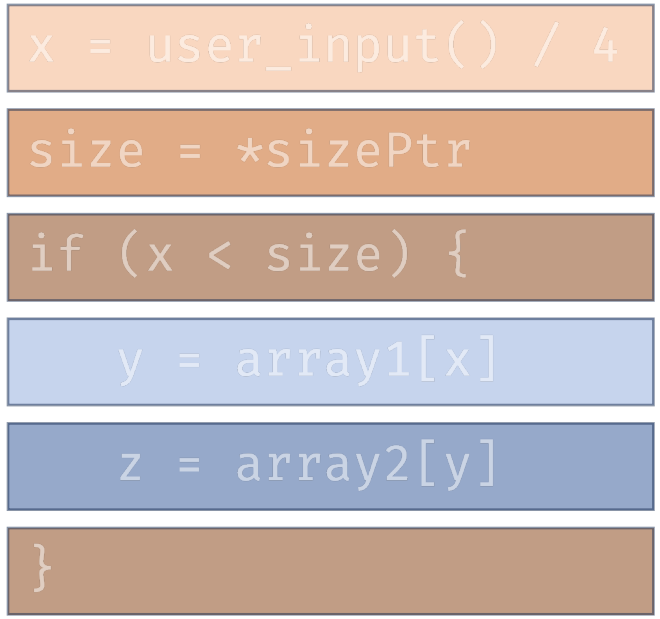
Step A: **Modelling** timing condition
Step B: **Simulating** windowing power
Step C: **Quantifying** exploitability

Our approach: An example



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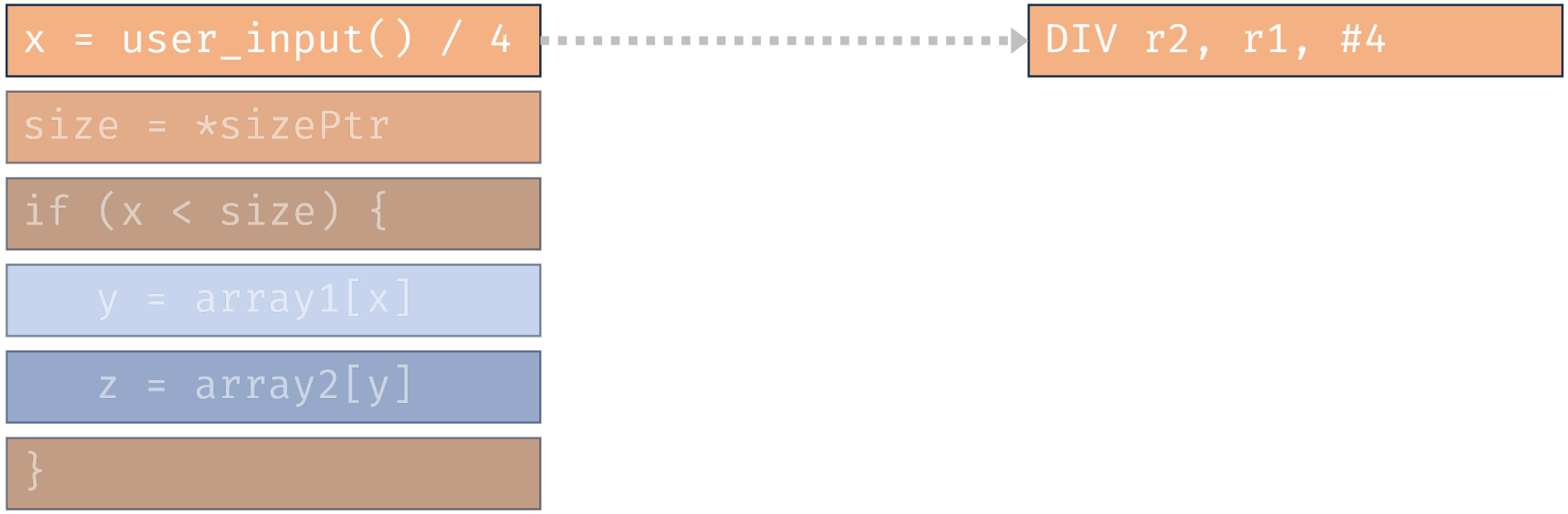

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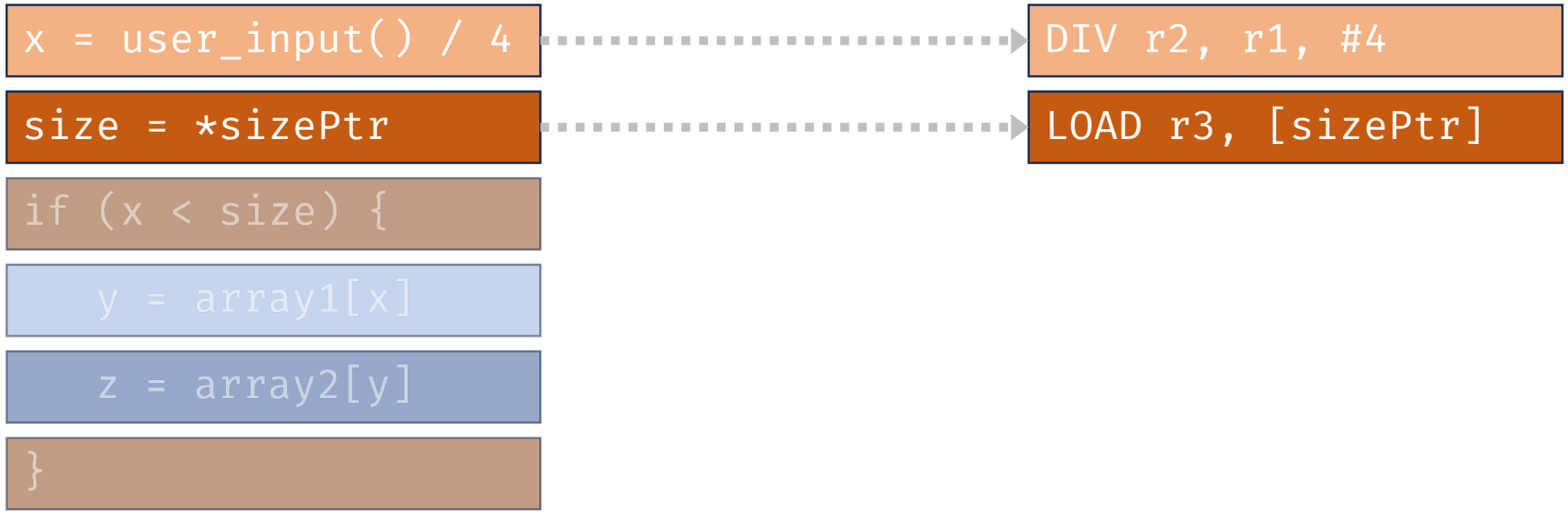

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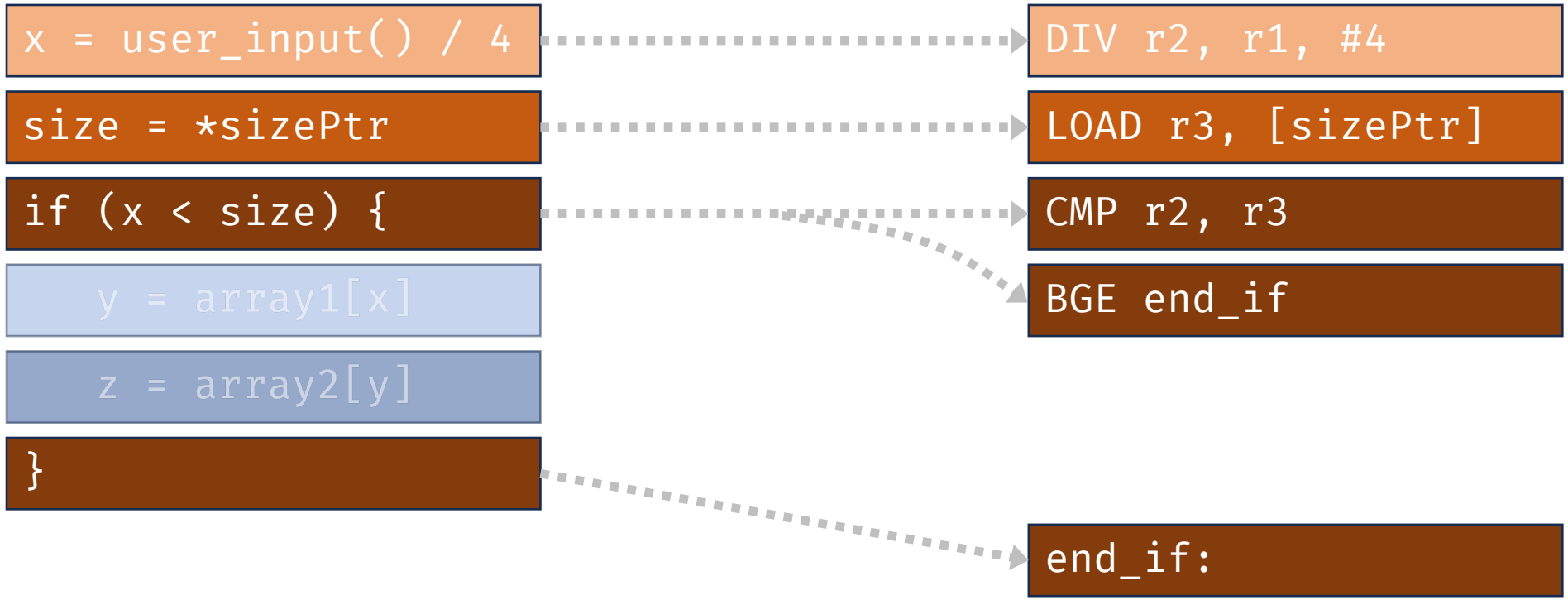

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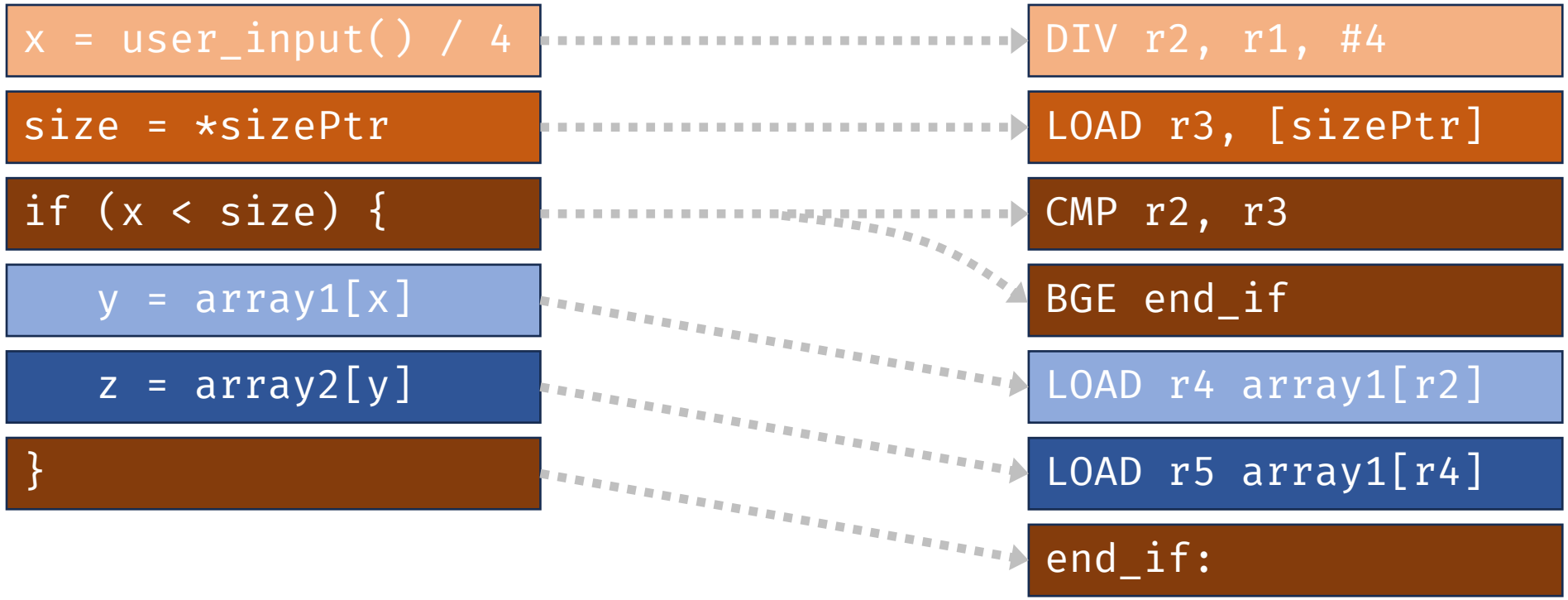
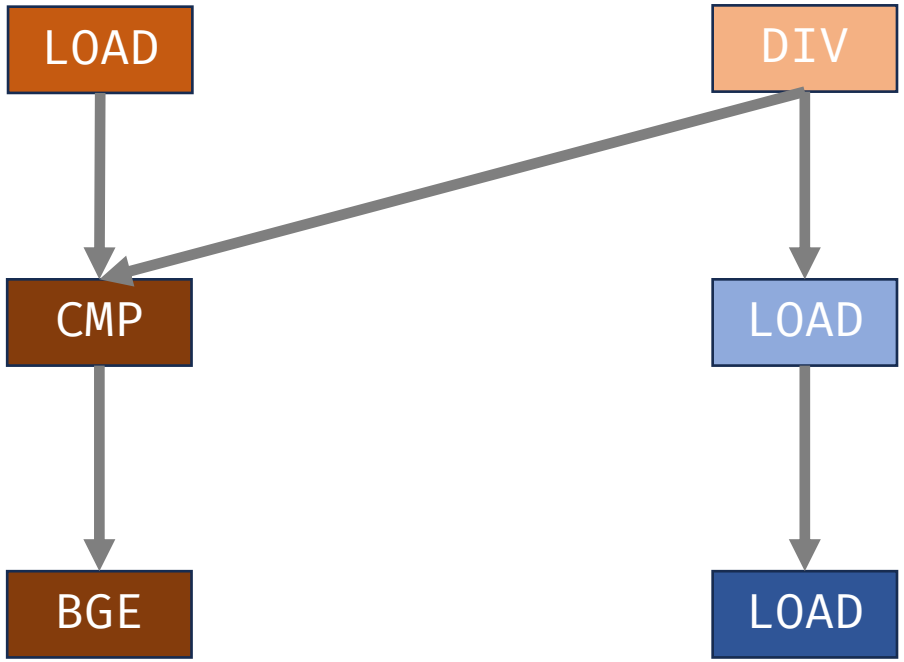


Step A: Modelling timing condition

```
DIV r2, r1, #4
LOAD r3, [sizePtr]
CMP r2, r3
BGE end_if
LOAD r4 array1[r2]
LOAD r5 array1[r4]
end_if:
```



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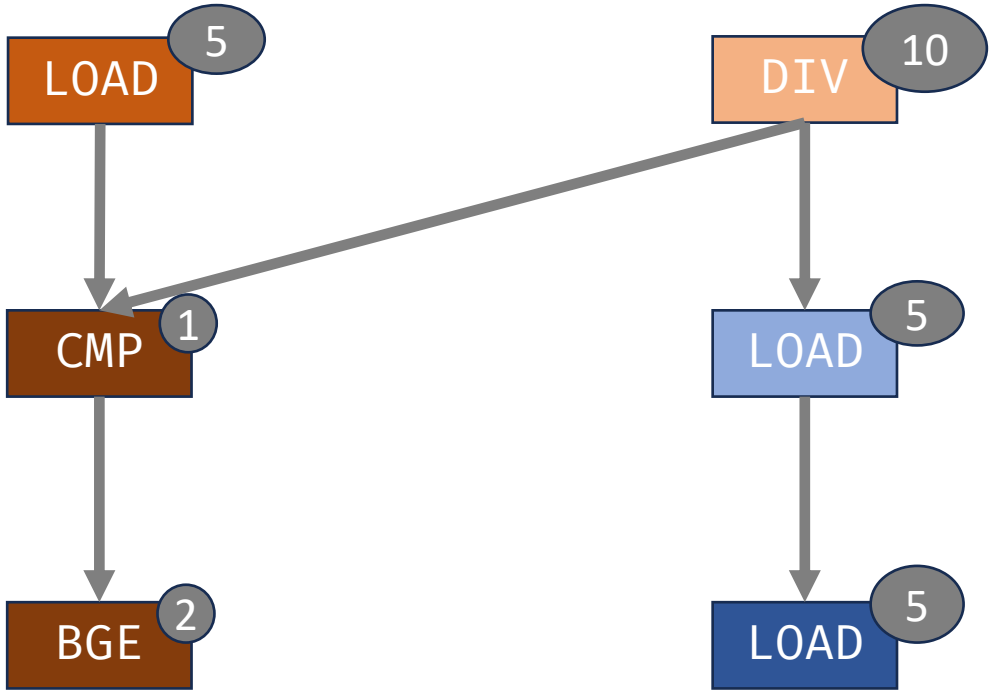

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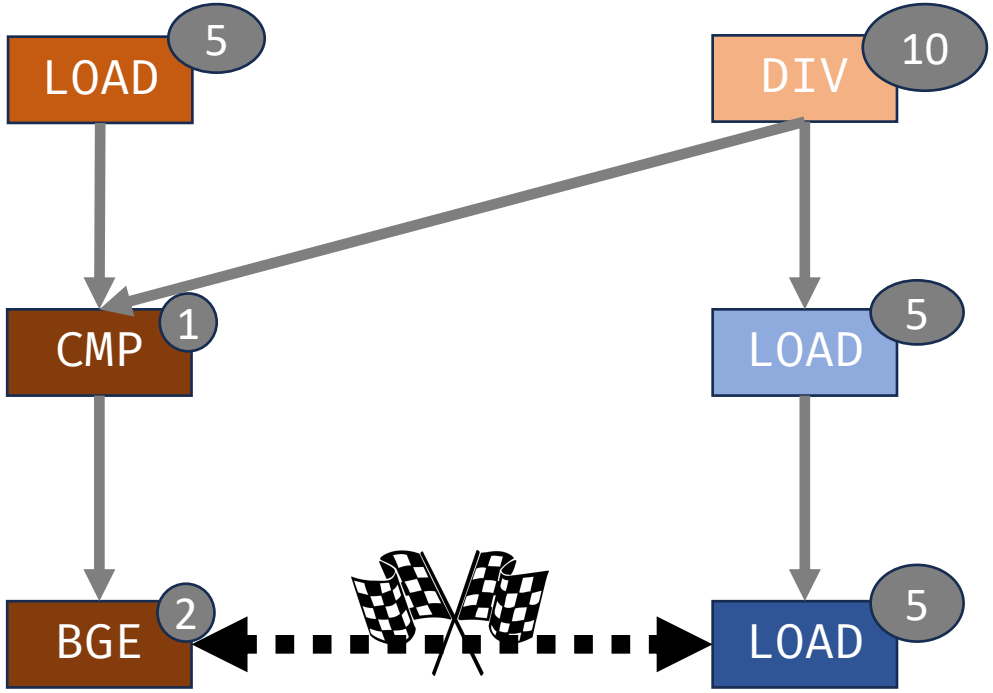

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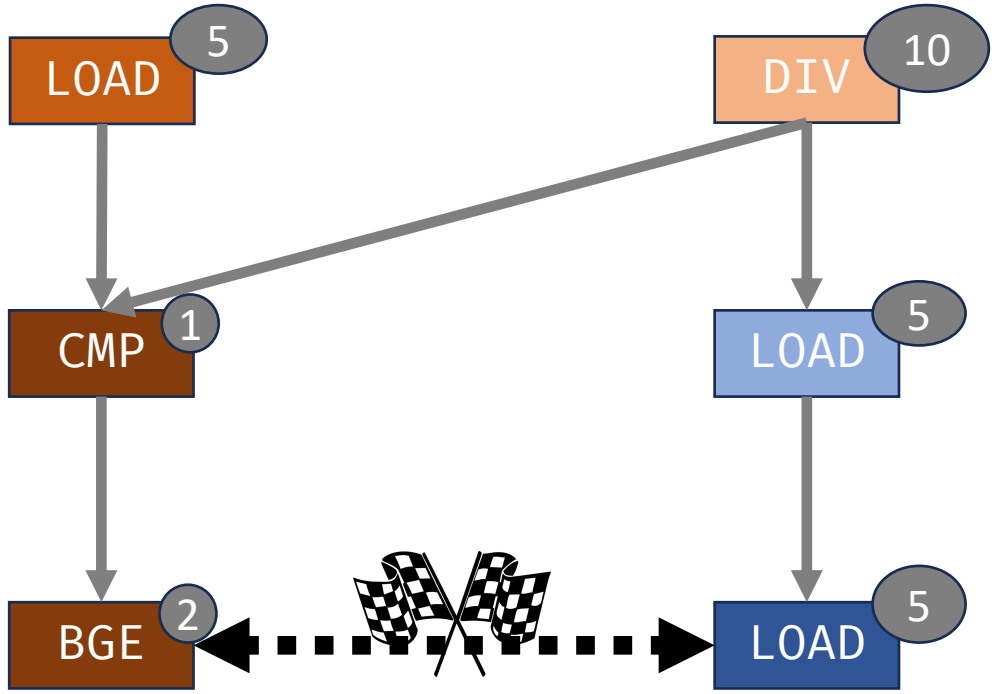

MaxPathWeight(BGE) — ***MaxPathWeight***(LOAD)

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```
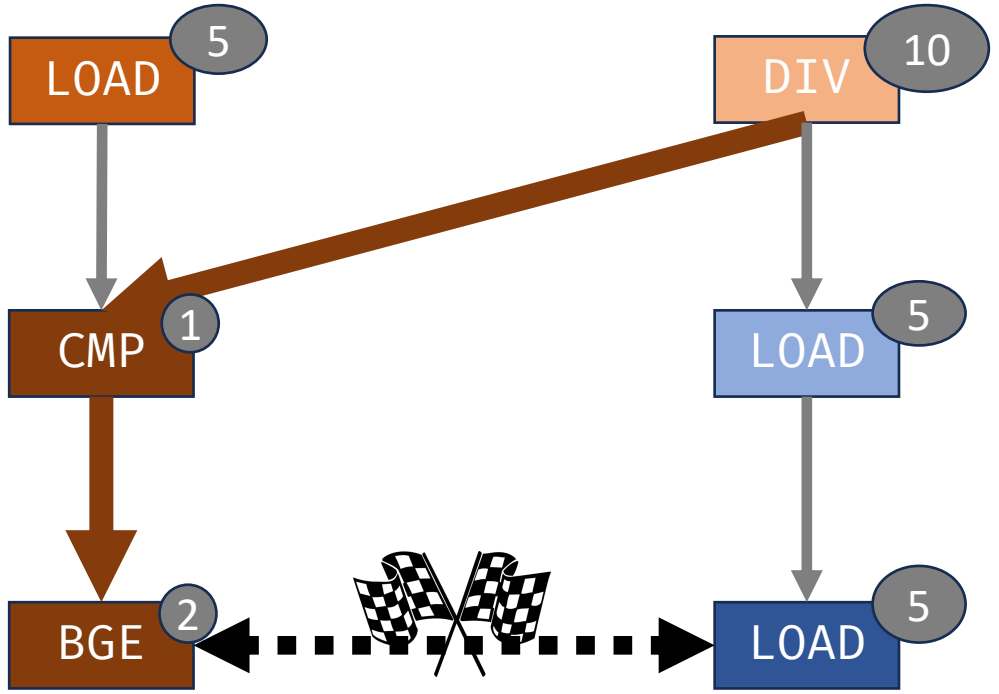
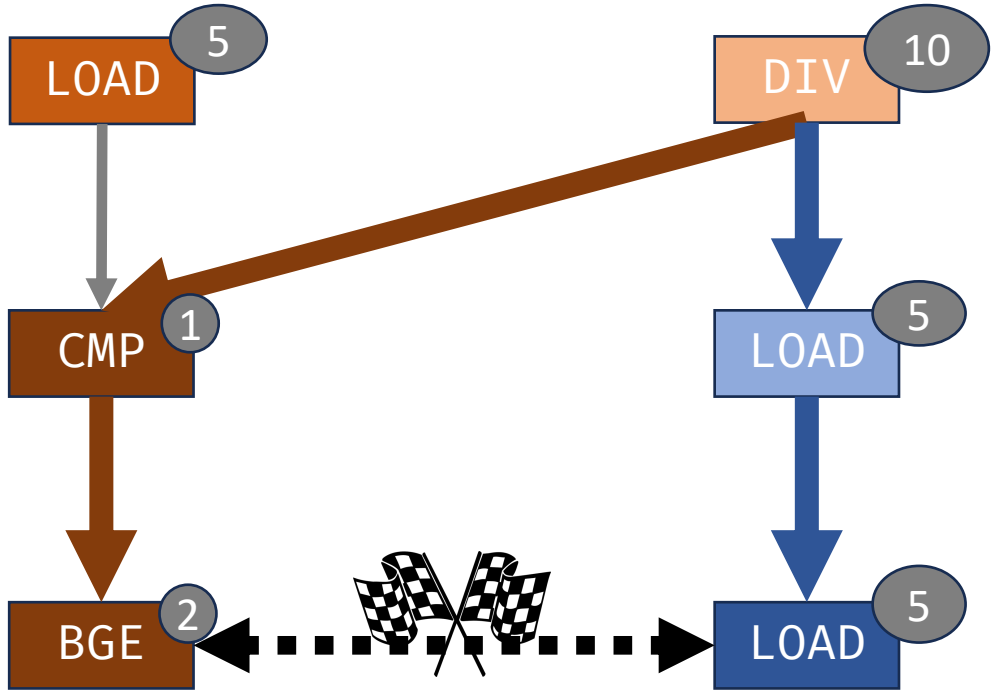



MaxPathWeight(BGE) — ***MaxPathWeight***(LOAD)

Step A: Modelling timing condition

```
DIV r2, r1, #4
LOAD r3, [sizePtr]
CMP r2, r3
BGE end_if
LOAD r4 array1[r2]
LOAD r5 array1[r4]
end_if:
```



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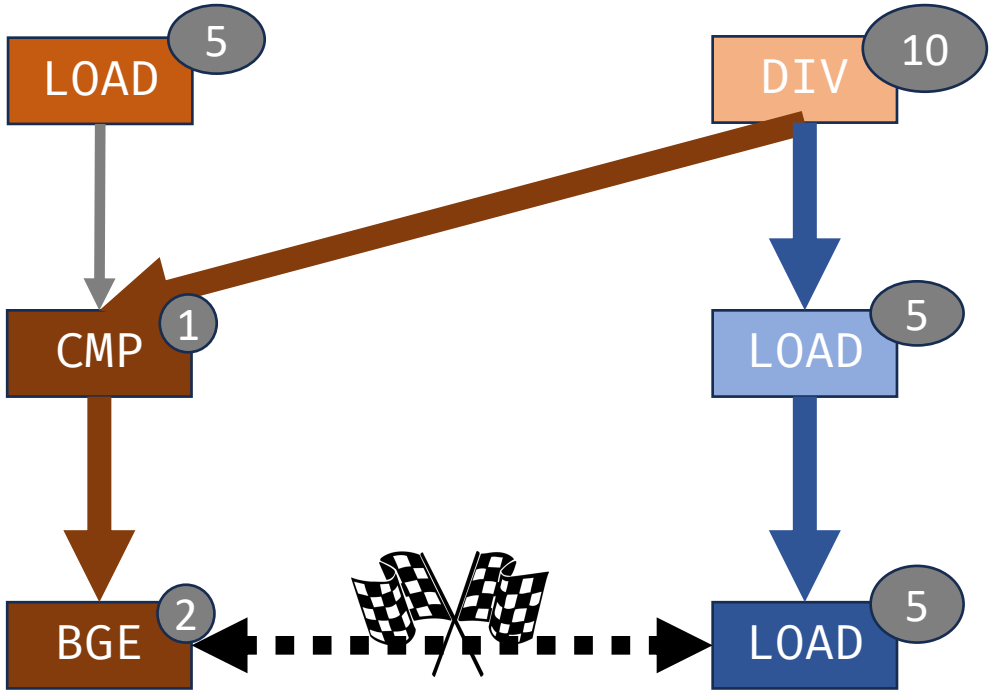
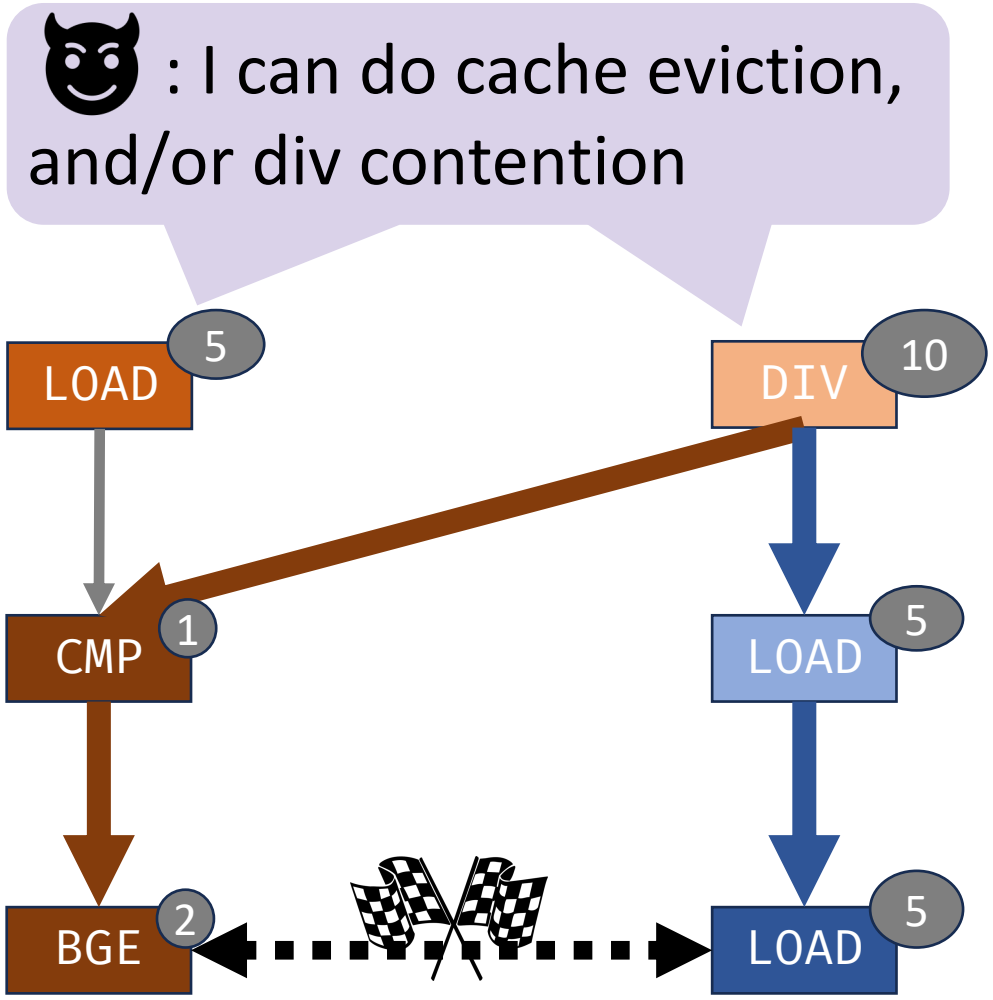


Timing Condition Index = ***MaxPathWeight***(BGE) − ***MaxPathWeight***(LOAD)

Step B: Simulating windowing power



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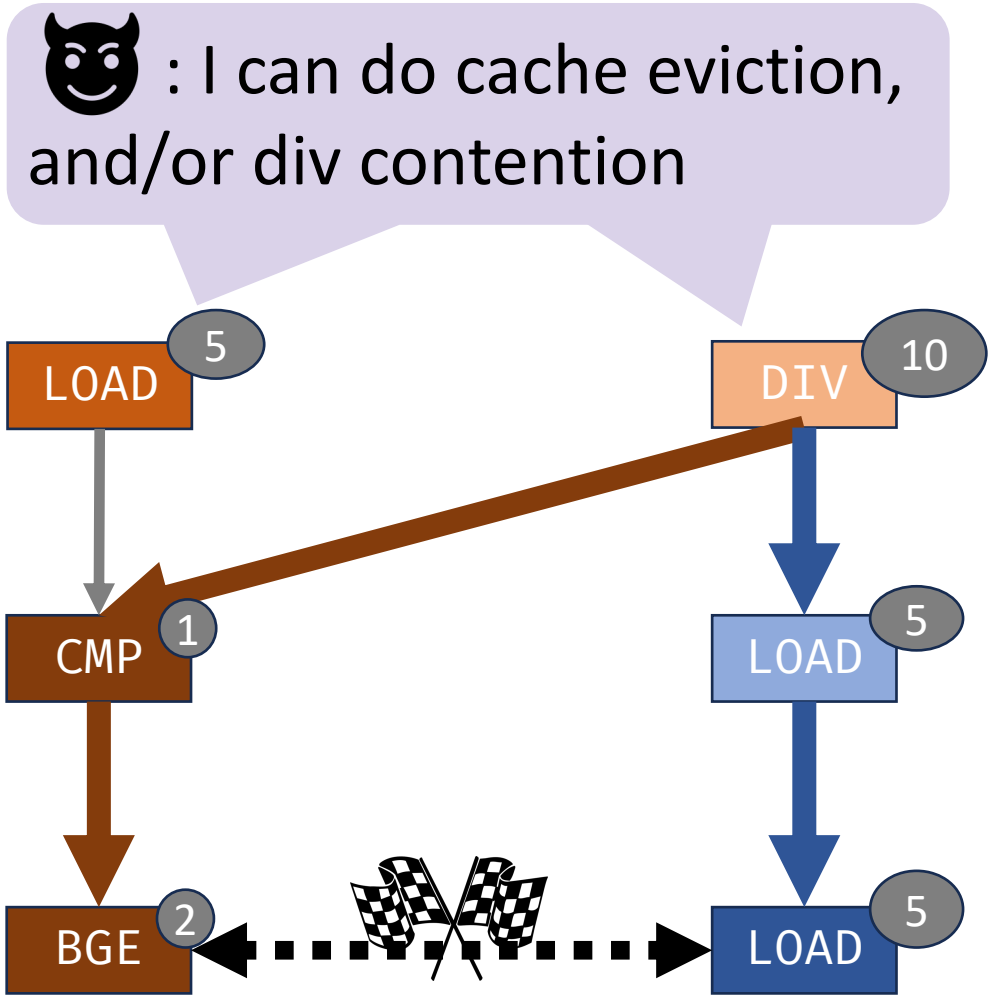
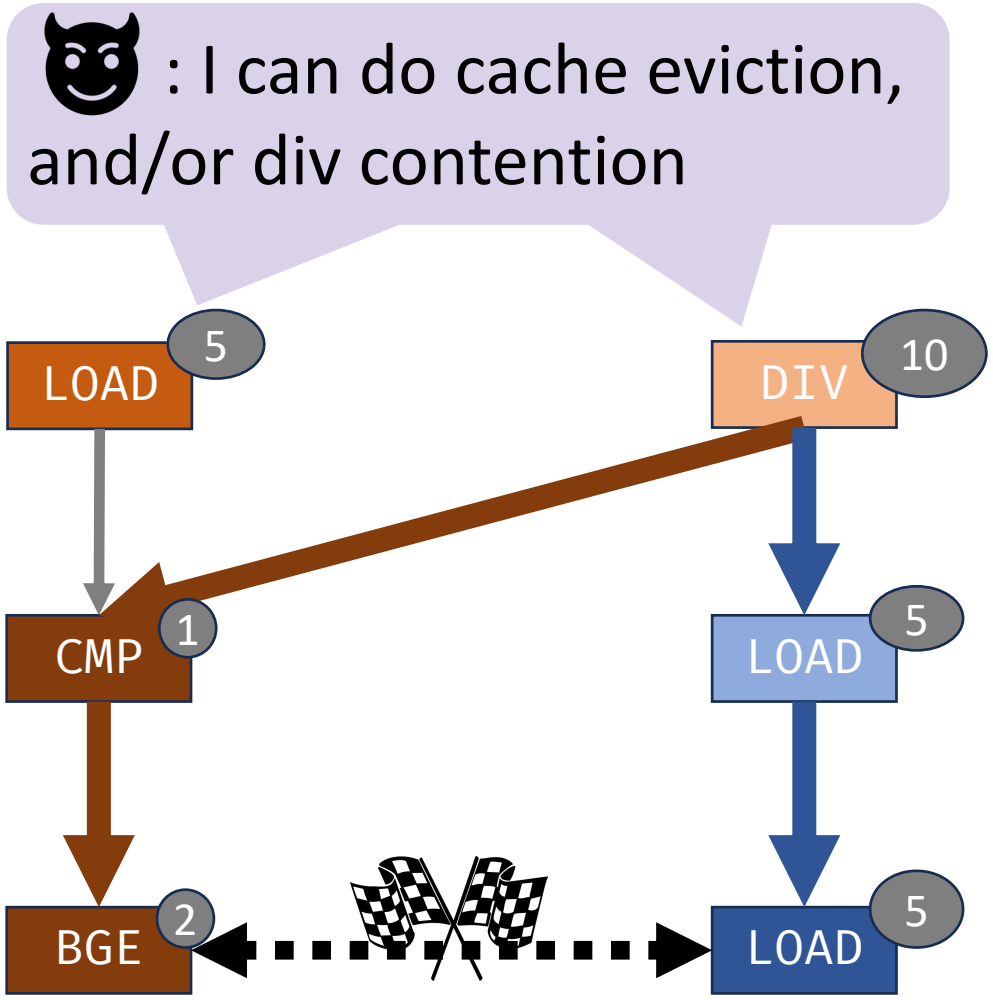


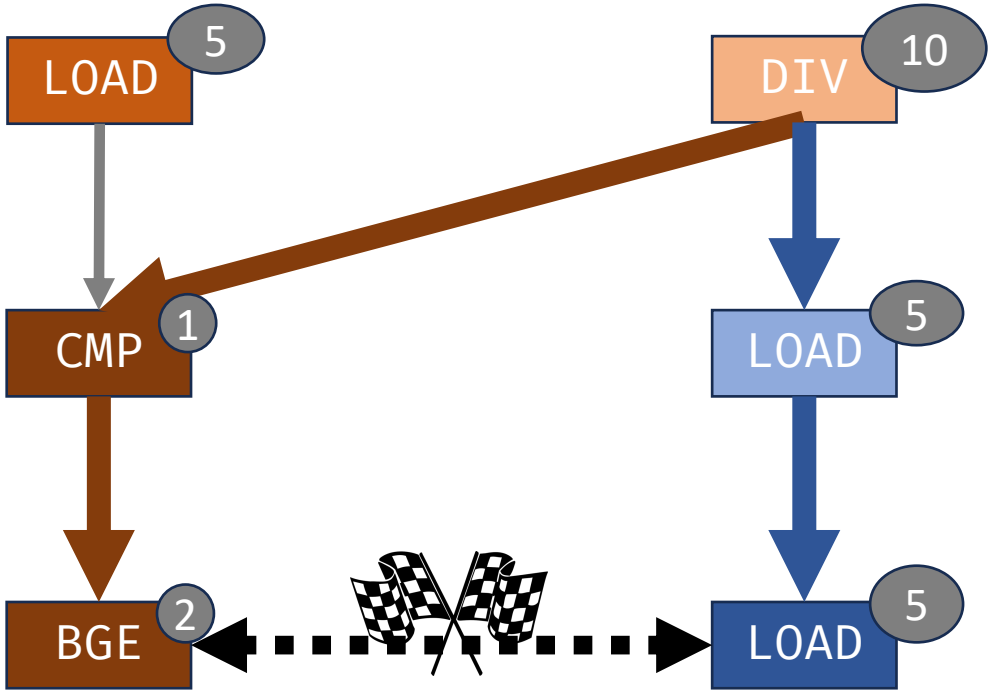
Attack Pattern
Do nothing
Cache eviction
Div contention
Cache eviction + Div contention

Step B: Simulating windowing power



Attack Pattern	Increase in Timing Condition Index
Do nothing	?
Cache eviction	?
Div contention	?
Cache eviction + Div contention	?

What if I do cache eviction?



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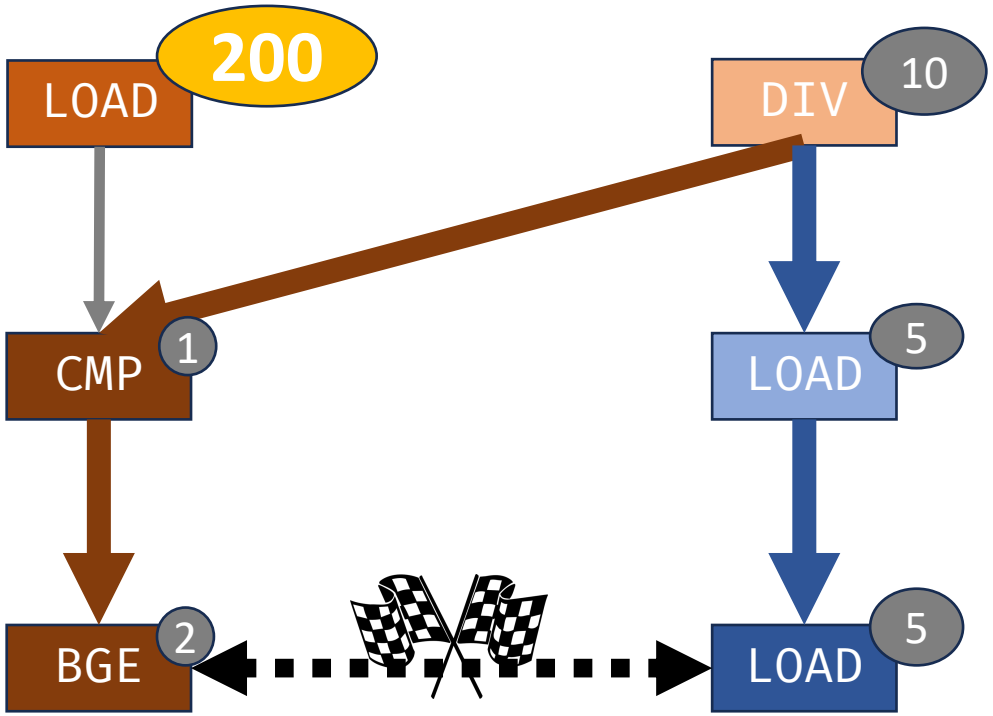

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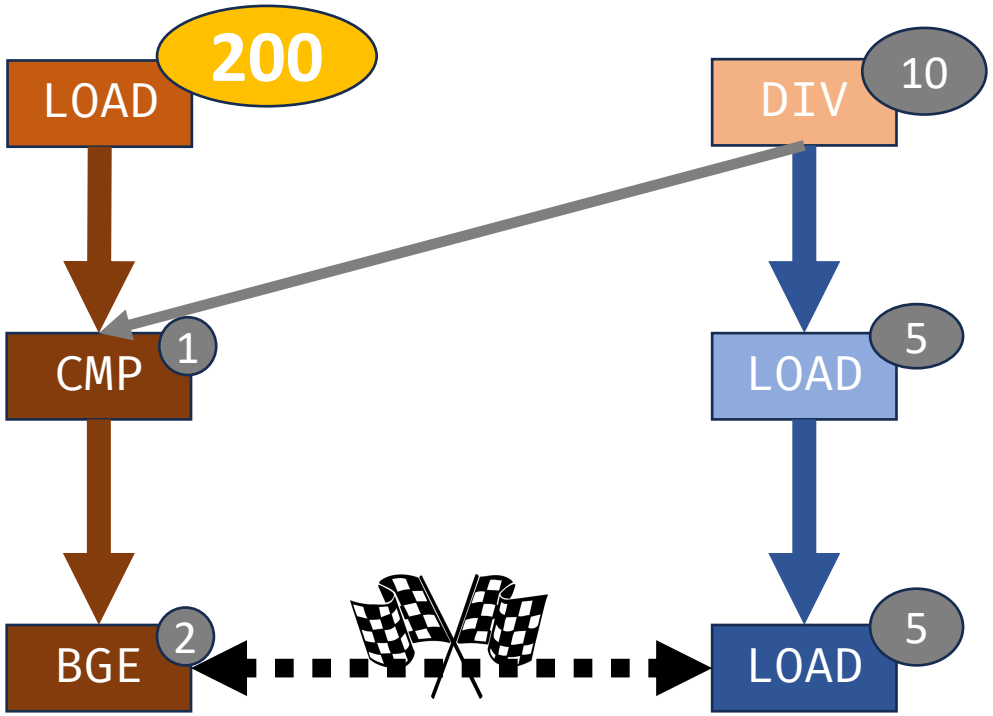

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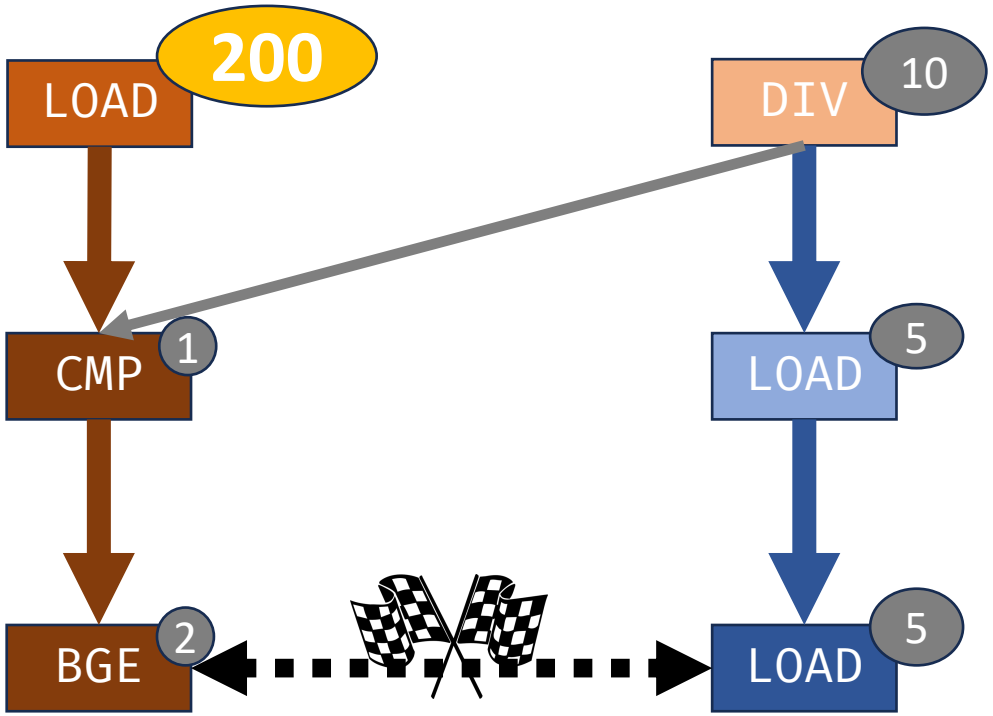
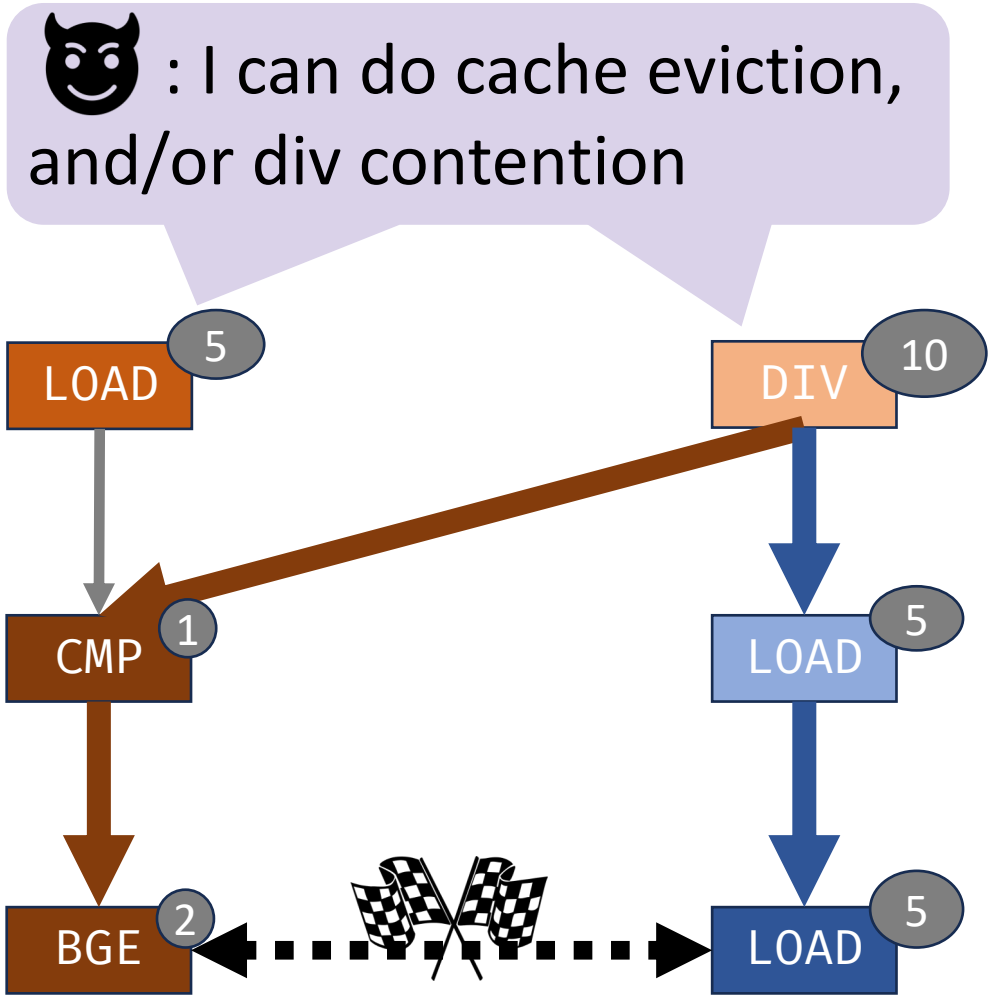


Timing Condition Index was -7.

Now, it increases to **183**!

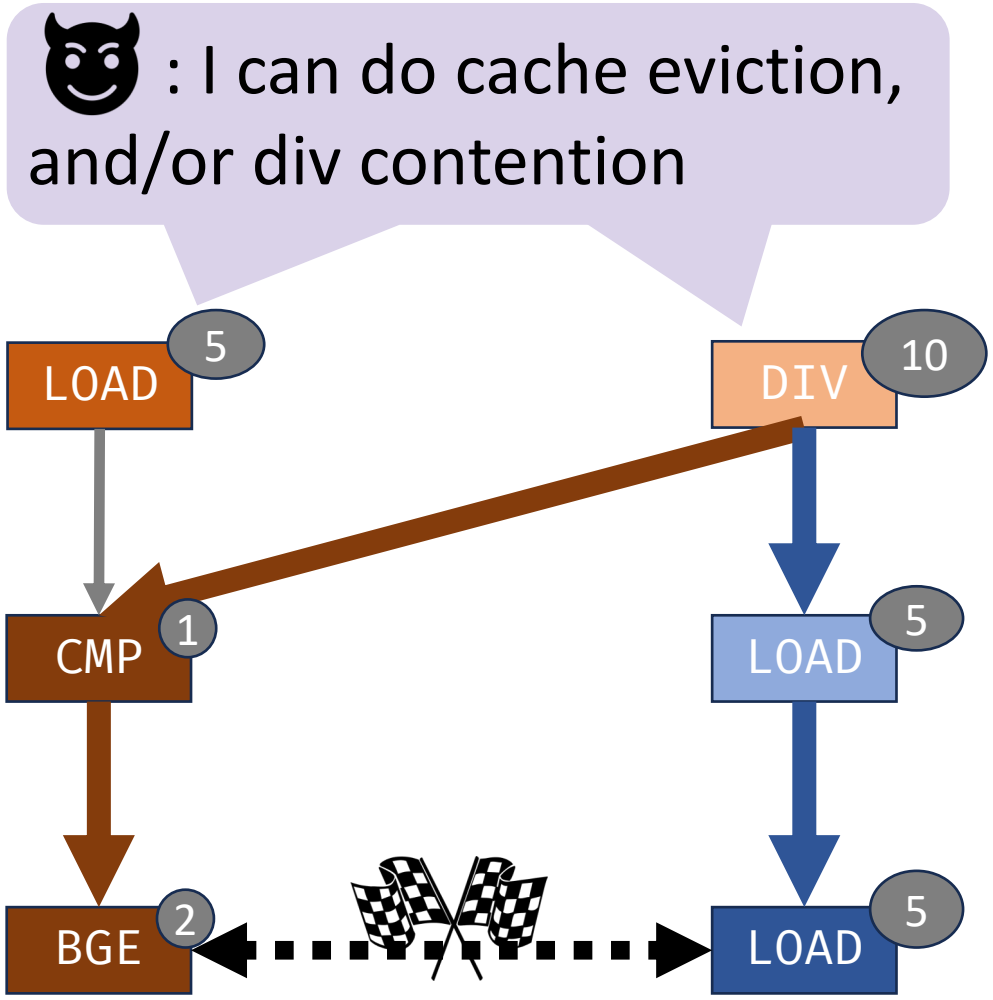
The attack pattern is effective :-)

Step B: Simulating windowing power



Attack Pattern	Increase in Timing Condition Index
Do nothing	0
Cache eviction	+190
Div contention	-140
Cache eviction + Div contention	+50

Step B: Simulating windowing power



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Step C: Measuring exploitability

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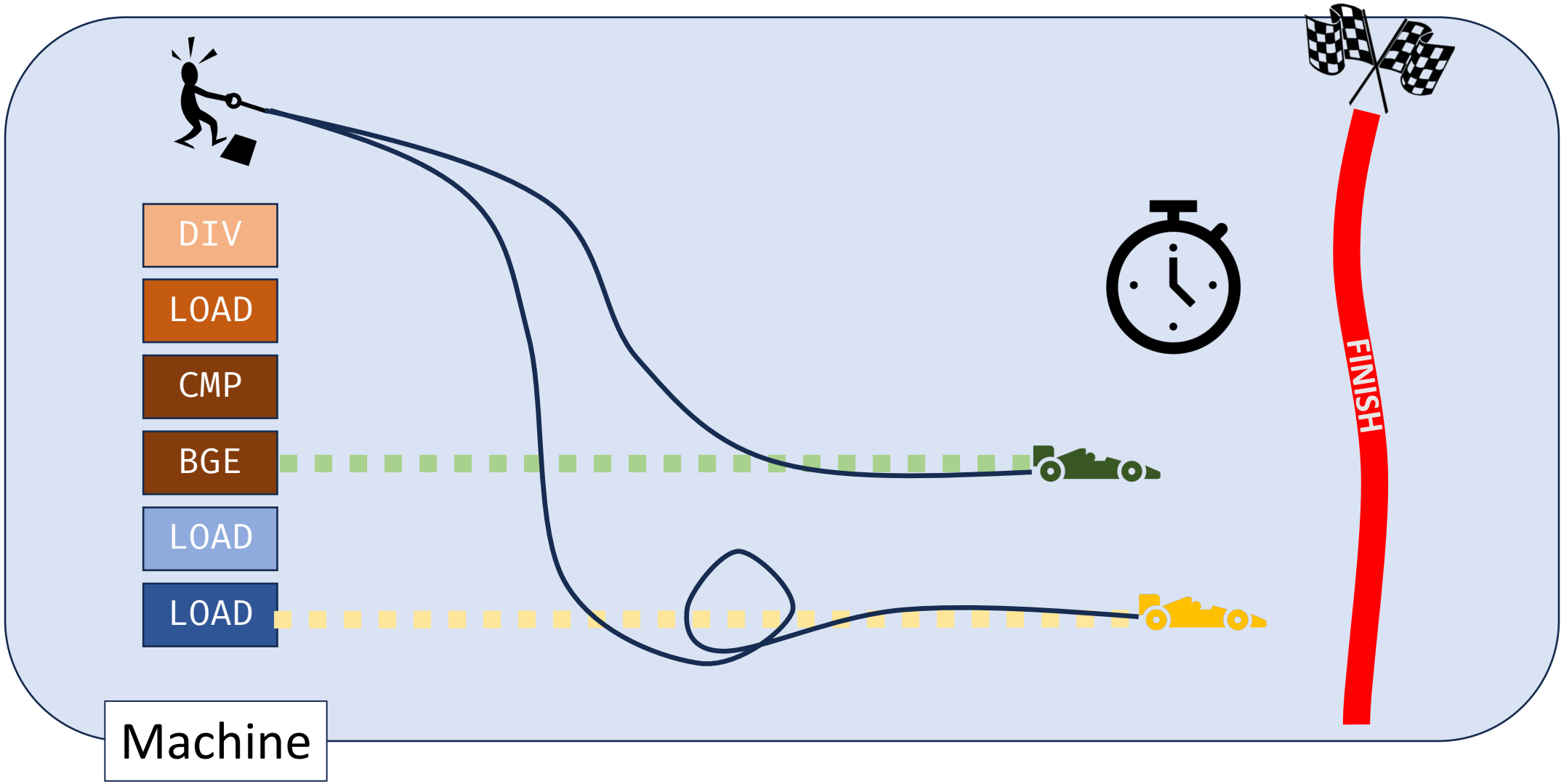

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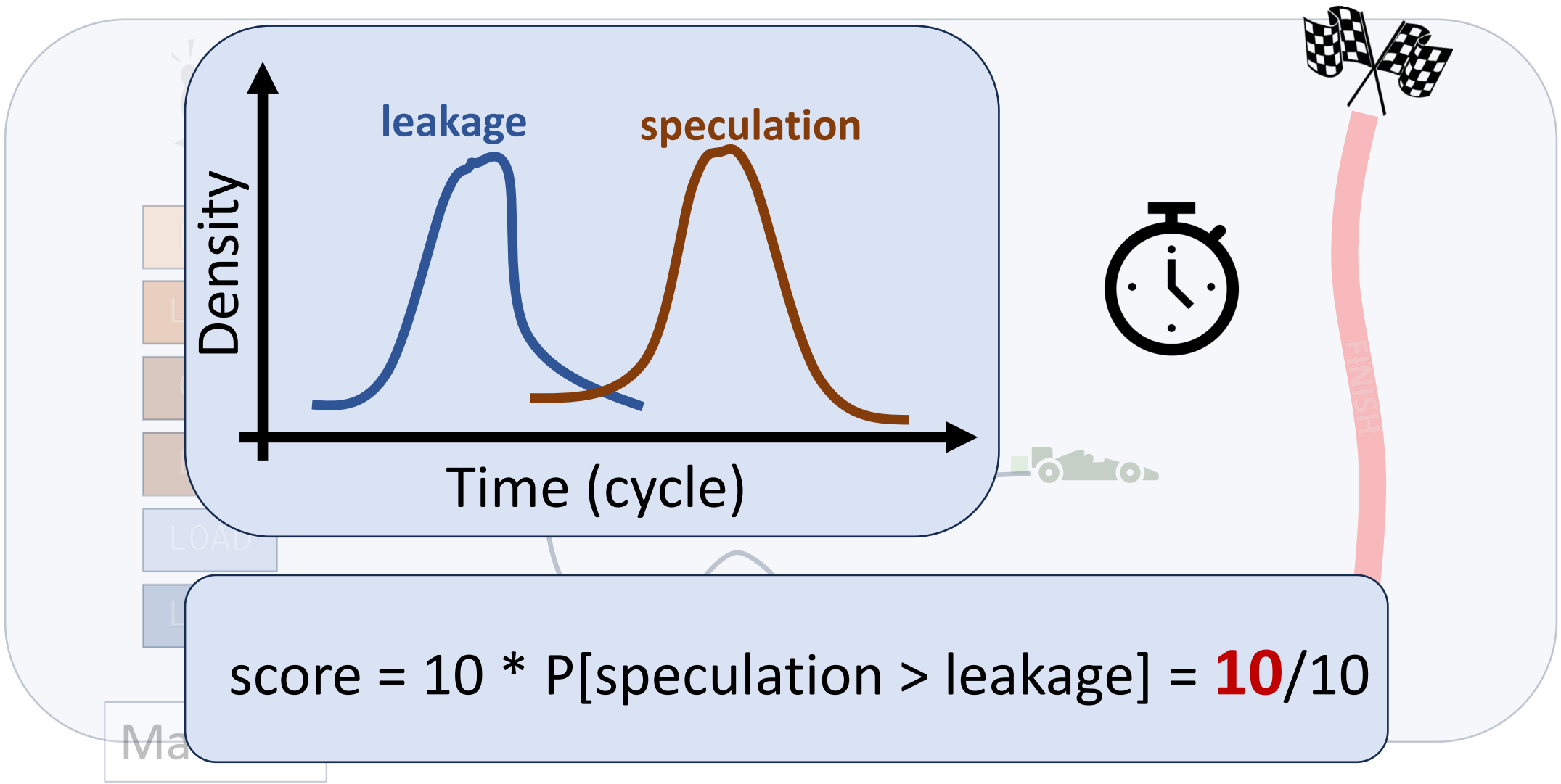
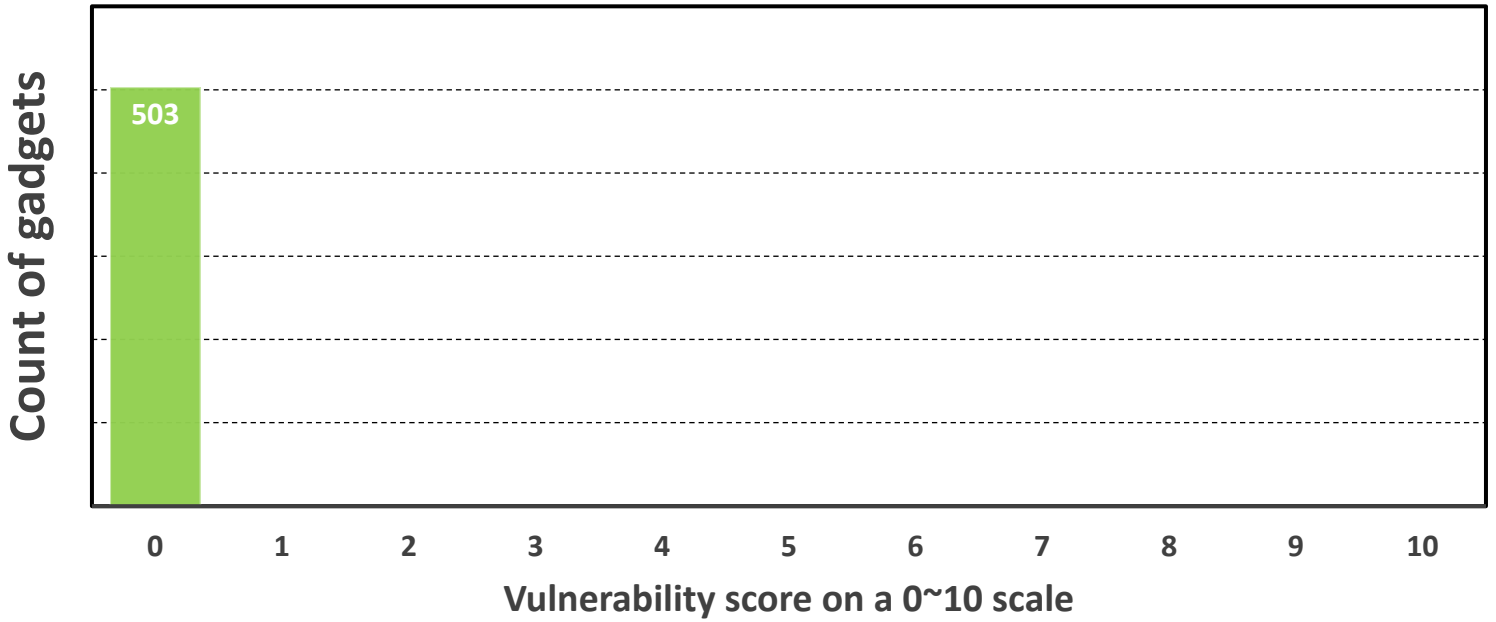
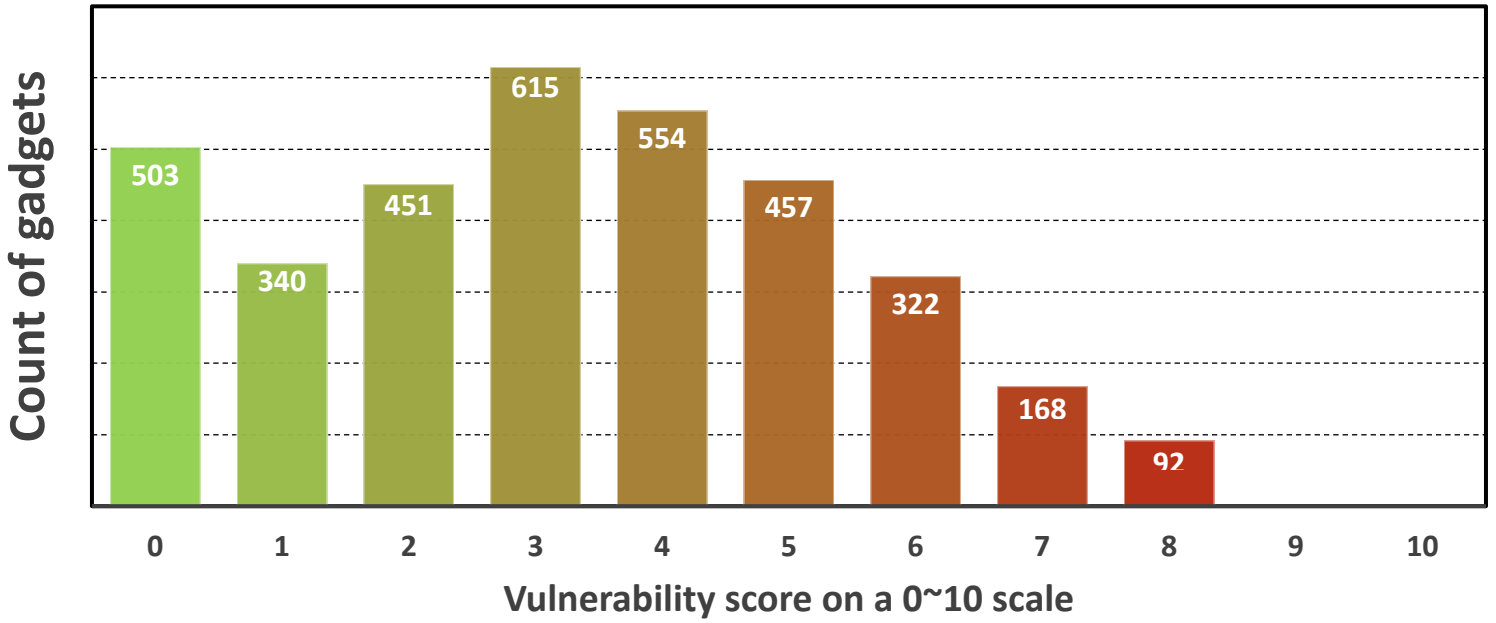


Evaluation: Gauging exploitability



- Target: gadgets with vulnerable information flow, identified by SOTA scanners.
- Applications: 6 security-centric applications and Linux kernel

Evaluation: Gauging exploitability



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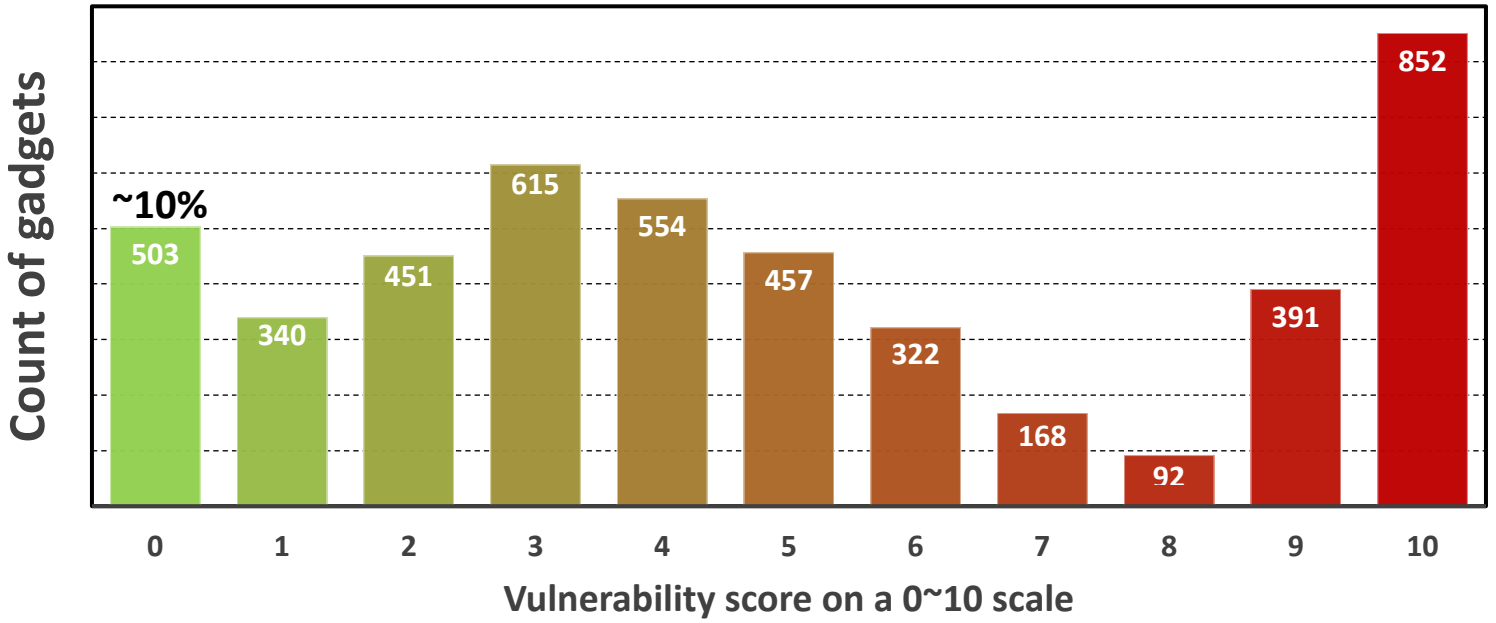

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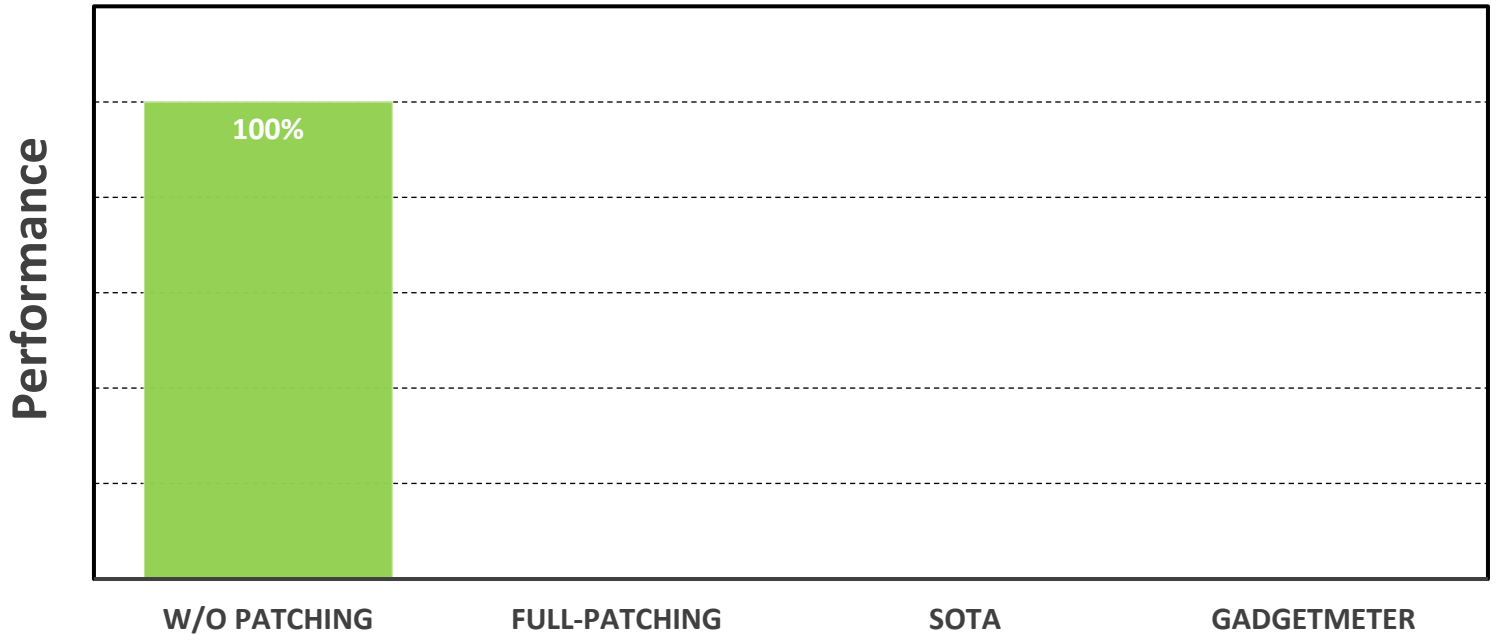
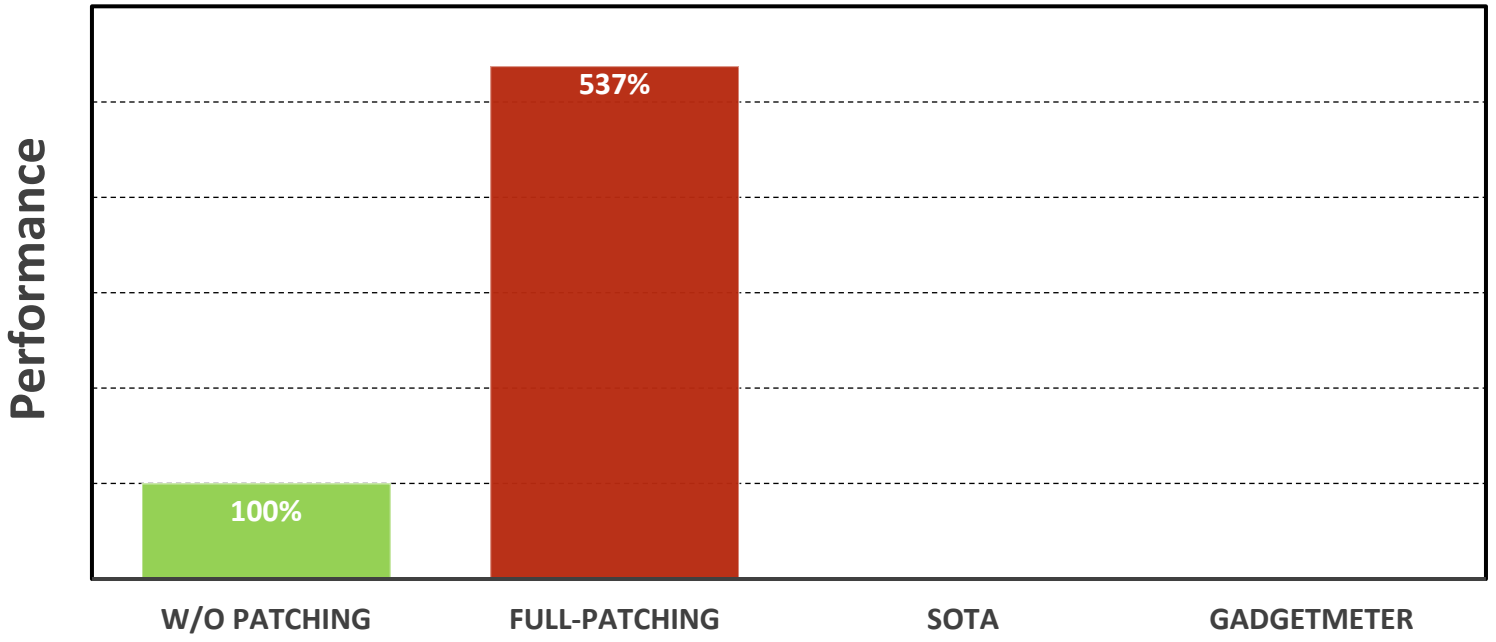
Evaluation: Performance improvement



- Patching method: LFENCE serialization.

Evaluation: Performance improvement



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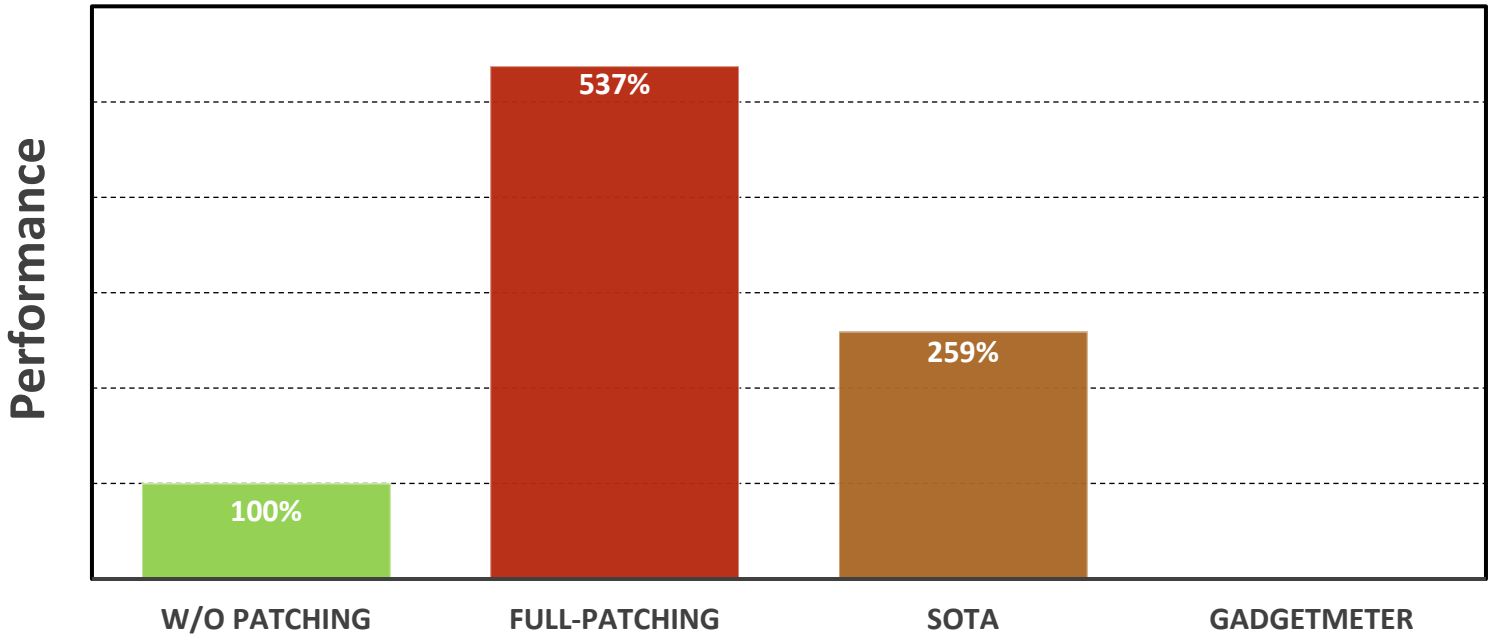

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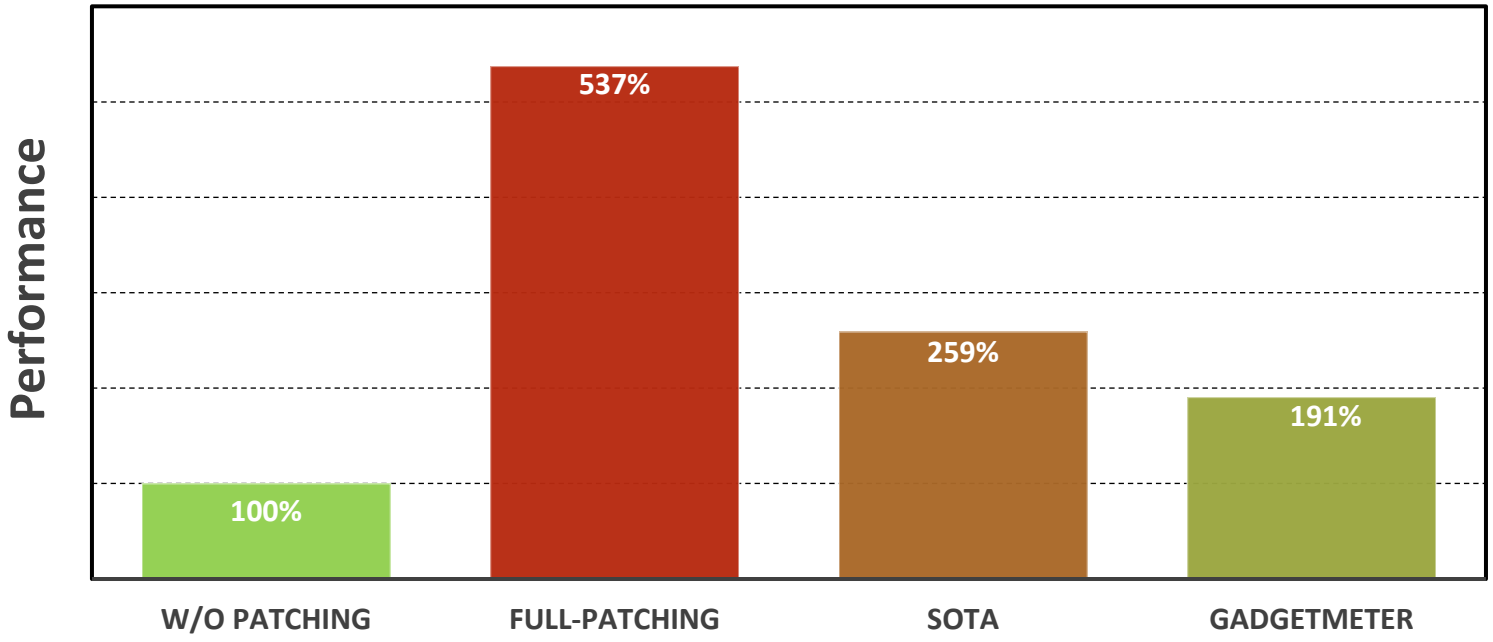
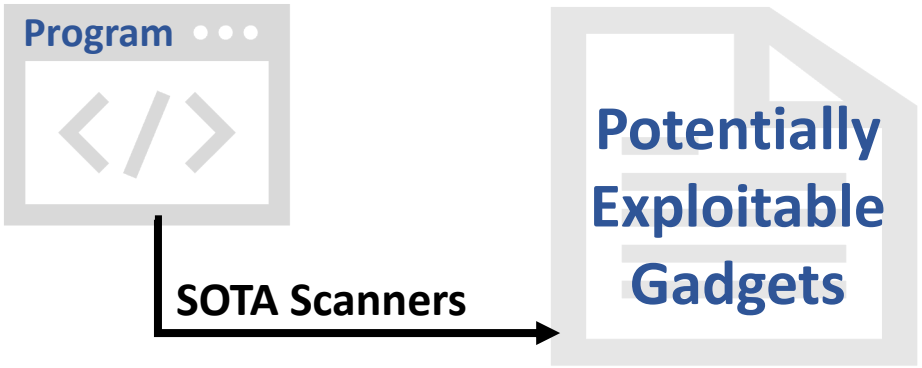


- Patching method: LFENCE serialization.
- Reduce overhead by 20.66%, compared with SOTA.

Conclusion

qiling07.github.io



- ✓ **Few** false negatives
- ✗ **Many** false positives
- ✗ **Binary** detection results

Conclusion

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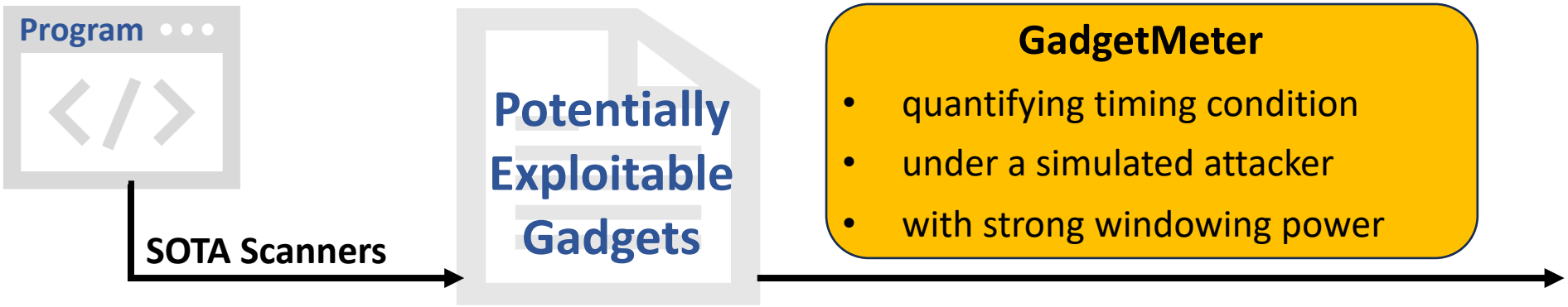

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