

# Poster: *HyPFuzz*: Formal-Assisted Processor Fuzzing

Chen Chen<sup>†</sup>, Rahul Kande<sup>†</sup>, Nathan Nguyen<sup>†</sup>, Flemming Andersen<sup>†</sup>, Aakash Tyagi<sup>†</sup>,  
Ahmad-Reza Sadeghi<sup>\*</sup>, and Jeyavijayan Rajendran<sup>†</sup>

<sup>†</sup>Texas A&M University, USA, <sup>\*</sup>Technische Universität Darmstadt, Germany

<sup>†</sup>{chenc, rahulkande, nathan.tm.nguyen, flandersen, tyagi, jv.rajendran}@tamu.edu,  
<sup>\*</sup>{ahmad.sadeghi}@trust.tu-darmstadt.de

## Abstract

Recent research has shown that hardware fuzzers can effectively detect security vulnerabilities in modern processors. However, existing hardware fuzzers do not fuzz well the hard-to-reach design spaces. Consequently, these fuzzers cannot effectively fuzz security-critical control- and data-flow logic in the processors, hence missing security vulnerabilities.

To tackle this challenge, we present *HyPFuzz*, a hybrid fuzzer that leverages formal verification tools to help fuzz the hard-to-reach part of the processors. To increase the effectiveness of *HyPFuzz*, we perform optimizations in time and space. First, we develop a scheduling strategy to prevent under- or over-utilization of the capabilities of formal tools and fuzzers. Second, we develop heuristic strategies to select points in the design space for the formal tool to target. We evaluate *HyPFuzz* on five widely-used open-source processors. *HyPFuzz* detected all the vulnerabilities detected by the most recent processor fuzzer and found three new vulnerabilities that were missed by previous extensive fuzzing and formal verification. This led to two new common vulnerabilities and exposures (CVE) entries. *HyPFuzz* also achieves  $11.68\times$  faster coverage than the most recent processor fuzzer.

## I. MAIN CONTENT

This research [1] is recently published in USENIX Security 2023. The original abstract and author list are shown above. We post the paper link with the conference version<sup>1</sup>.

## REFERENCES

- [1] C. Chen, R. Kande, N. Nguyen, F. Andersen, A. Tyagi, A.-R. Sadeghi, and J. Rajendran, “HyPFuzz: Formal-Assisted Processor Fuzzing,” *USENIX Security Symposium*, pp. 1361–1378, 2023.

<sup>1</sup><https://www.usenix.org/conference/usenixsecurity23/presentation/chen-chen>



TEXAS A&M UNIVERSITY



TECHNISCHE UNIVERSITÄT DARMSTADT

# HyPFuzz: Formal-Assisted Processor Fuzzing

Chen Chen<sup>†</sup>, Rahul Kande<sup>†</sup>, Nathan Nyugen<sup>†</sup>, Flemming Andersen<sup>†</sup>, Aakash Tyagi<sup>†</sup>, Ahmad-Reza Sadeghi<sup>\*</sup>, and Jeyavijayan Rajendran<sup>†</sup>  
<sup>†</sup>Texas A&M University, <sup>\*</sup>Technische Universität Darmstadt



## Introduction

- Hardware vulnerabilities are difficult to be patched.
- Hardware vulnerabilities emerge at an alarming rate.

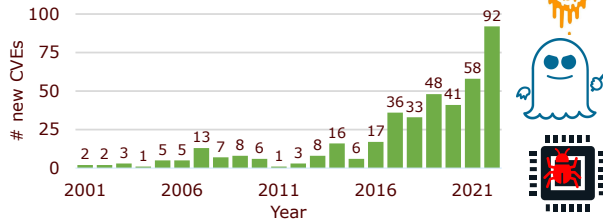


Figure 1. Exponential increase in the number of hardware vulnerabilities [1].

## Research Objective

- HyPFuzz, a hybrid fuzzer that leverages formal verification tools to help fuzz the hard-to-cover part of the processors.

Technique	Automated	Scalable	Efficient	Coverage
Manual Inspection	✗	✗	✗	✗
Formal verification	✗	✗	✓	✗
Random regression	✓	✓	✗	✗
Hardware Fuzzing	✓	✓	✓	✗
HyPFuzz	✓	✓	✓	✓

Table 1. Comparison between various hardware verification techniques.

## Methodology

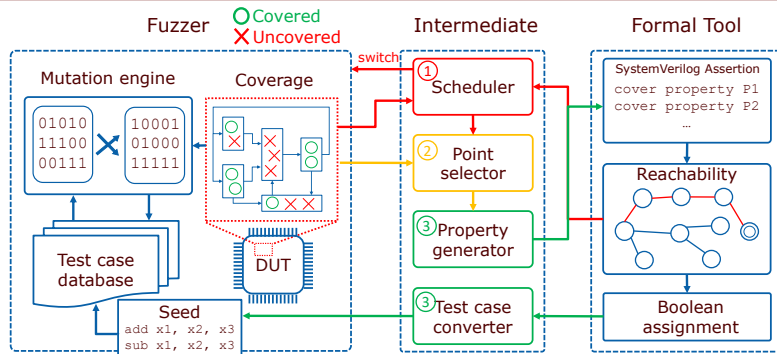


Figure 2. Framework of HyPFuzz.

### Challenge 1: Scheduling of Fuzzer and Formal Tool

- Switch from fuzzer to formal when  $r_{fuzz}(w) < r_{fml}$ .
- Rate of fuzzer of the recent  $w$  tests:  $r_{fuzz}(w) = \frac{\text{total new cov.}(w)}{\text{total simtime}(w)}$
- Rate for formal tool of  $|C|$  points selected:  $r_{fml} = \frac{\text{num.of points in } C}{\text{total proof time}}$

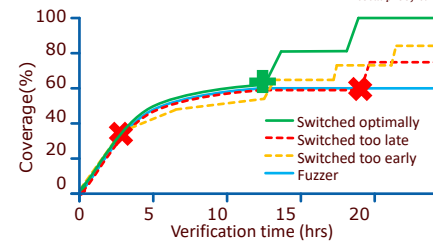


Figure 3. Switch illustration from fuzzer to formal tool.

### Challenge 2: Selection of Uncovered Points

- BotTop** selects modules with the deepest distance to the top module.
- MaxUnconvd** selects modules with the maximal number of uncovered points.
- ModDep** selects modules with the highest logic dependence.

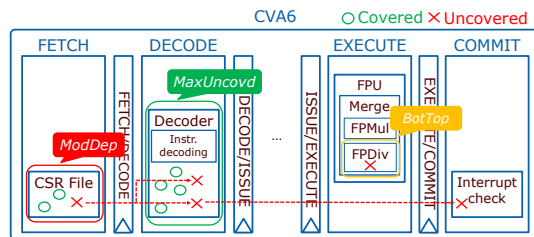


Figure 4. Different point selection strategies on CVA6[3].

### Challenge 3: Seamless Integration

#### Property generator

```
// Interrupt handler
if (mie[S_TIMER_INTERRUPT] == mip[S_TIMER_INTERRUPT])
  interrupt_cause = S_TIMER_INTERRUPT; // Supervisor timer
if (mie[S_SW_INTERRUPT] == mip[S_SW_INTERRUPT])
  interrupt_cause = S_SW_INTERRUPT; // Supervisor Software
if (mie[S_EXT_INTERRUPT] == mip[S_EXT_INTERRUPT] | irq[
  → SupervisorIrq])
  interrupt_cause = S_EXT_INTERRUPT; // Supervisor External
```

An uncovered branch point

Conditions

```
cover property (mie[S_SW_INTERRUPT]
  && mip[S_SW_INTERRUPT])
```

The corresponding SVA property

#### Test case converter



Boolean assignments

Instructions

Template(Binary)	Valid file(Binary)
0x80000000	0x00000113
0x8000258c	0x8000258c
0x80002590	0x00000113
0x80002594	0x80002594
0x80002598	0x00000113

Seed

## Experiment

### Vulnerability detection

- Detected existing 11 vulnerabilities 3.06 × less time.
- Detected three new vulnerabilities.
- Resulted two CVEs: CVE-2022-33021, CVE-2022-33023.

### Branch coverage achievement compared to:

- TheHuzz[2]: 41.24x speedup, 6.84% more total coverage.
- Random regression: 239.93x speedup, 12.70% more total coverage.

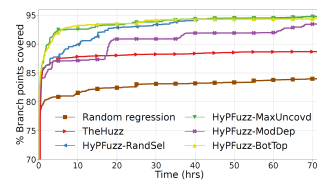


Figure 5. Branch points achieved by random regression, TheHuzz[2], and HyPFuzz on CVA6[3].

## Reference

- National Vulnerability Database. <https://nvd.nist.gov/>, 2023.
- Kande, Rahul, et al. "TheHuzz: Instruction Fuzzing of Processors Using Golden-Reference Models for Finding Software-Exploitable Vulnerabilities." USENIX Security, 2022.
- Zaruba, Florian, et al. "The Cost of Application-Class Processing: Energy and Performance Analysis of a Linux-Ready 1.7-GHz 64-Bit RISC-V Core in 22-nm FDSOI Technology." VLSI, 2019.

### Contact

- Chen Chen, Ph.D. student in Computer Engineering, Texas A&M University
- Email: [chenc@tamu.edu](mailto:chenc@tamu.edu) Lab Website: <https://seth.engr.tamu.edu/>