SCIENCE
PASSION
TECHNOLOGY

Memory Band-Aid

A Principled Rowhammer Defense-in-Depth

Carina Fiedler, Jonas Juffinger, Sudheendra Raghav Neela, Martin Heckel, Hannes Weissteiner, Abdullah Giray Yağlıkçı, Florian Adamsky, and Daniel Gruss

Graz University of Technology

NDSS 2026

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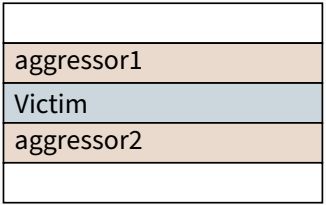
Rowhammer

- Hardware fault of the DRAM



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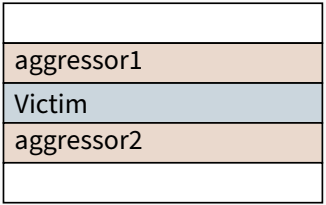

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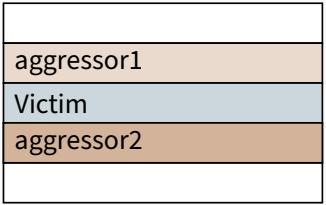

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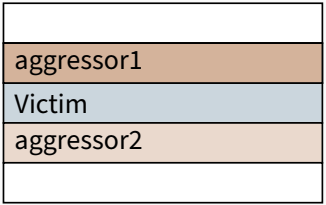

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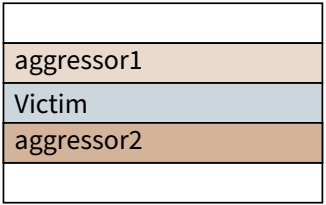

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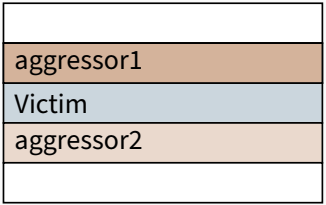

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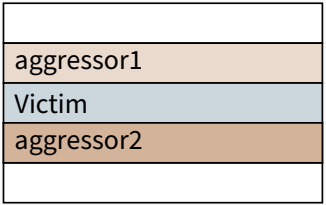

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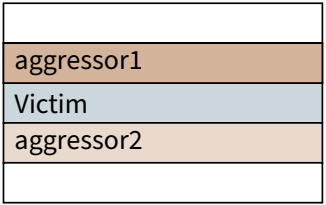

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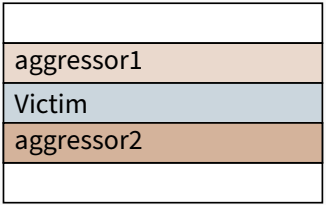

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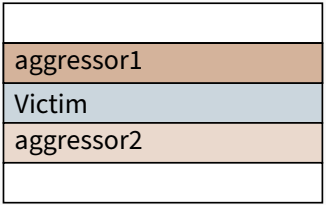

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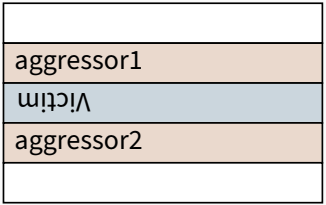

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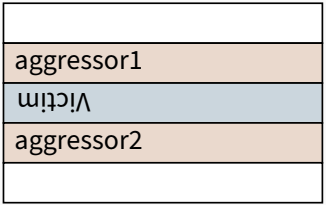

Rowhammer

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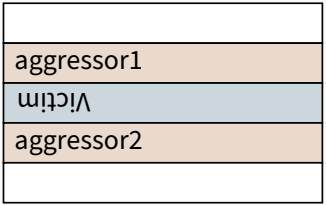
- Worse with every new DRAM generation
- Enables attacks, many countermeasures proposed



Reaching DRAM

- Cache stores data on access

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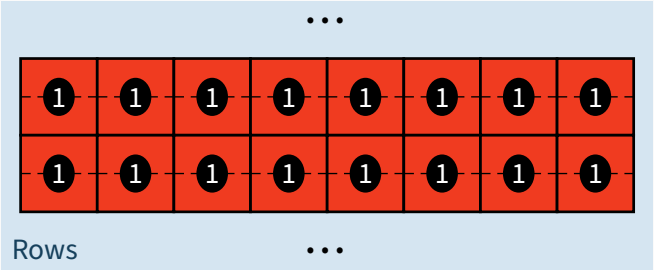
- `clflush` instruction removes data from cache

Reaching DRAM

- Cache stores data on access
- `clflush` instruction removes data from cache
- Flush+Reload loop

```
for (i = 0; i < N; ++i) {
  *aggressor1;
  *aggressor2;
  flush(aggressor1);
  flush(aggressor2);
}
```

Cell Discharge



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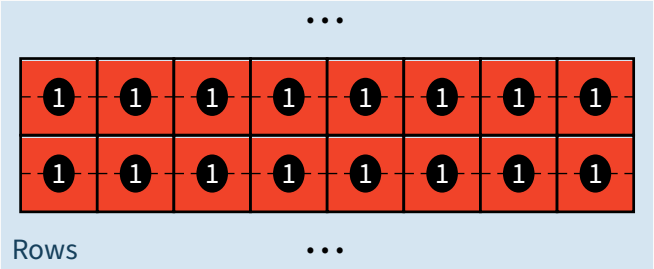

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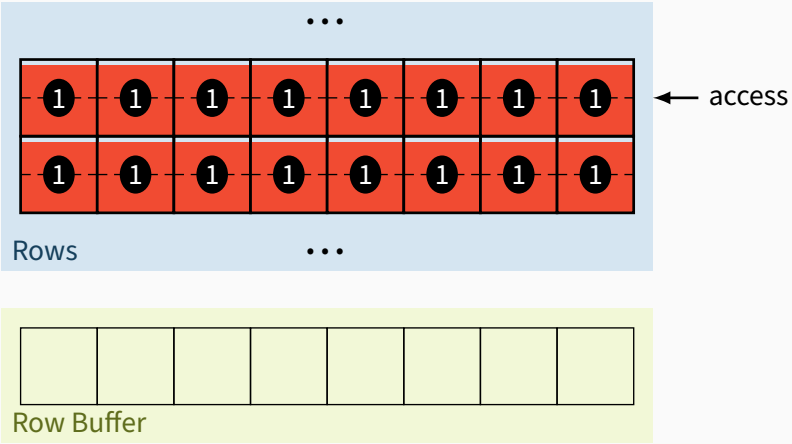

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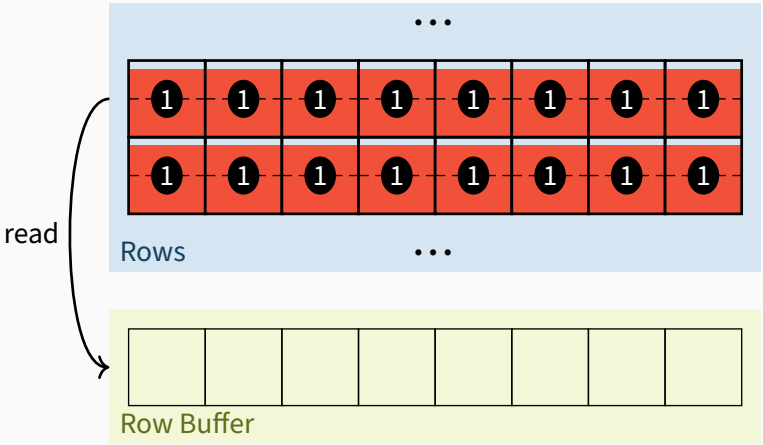

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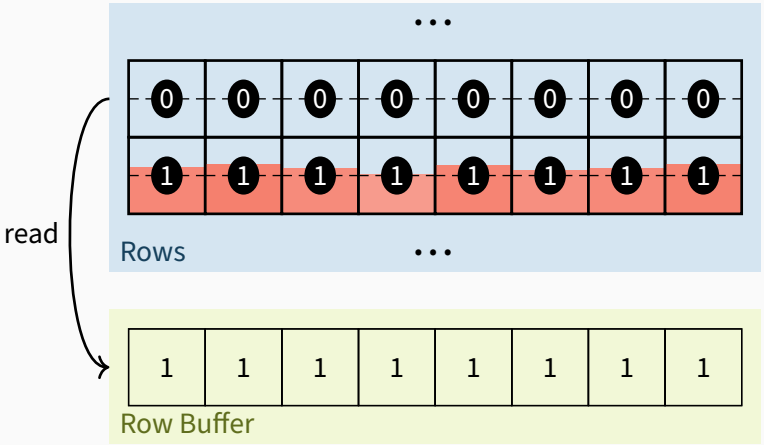

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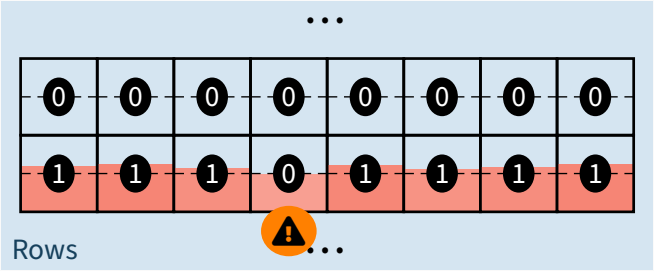

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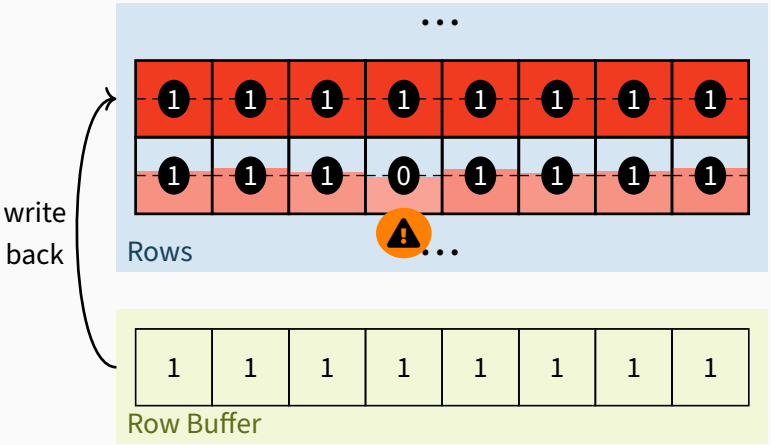

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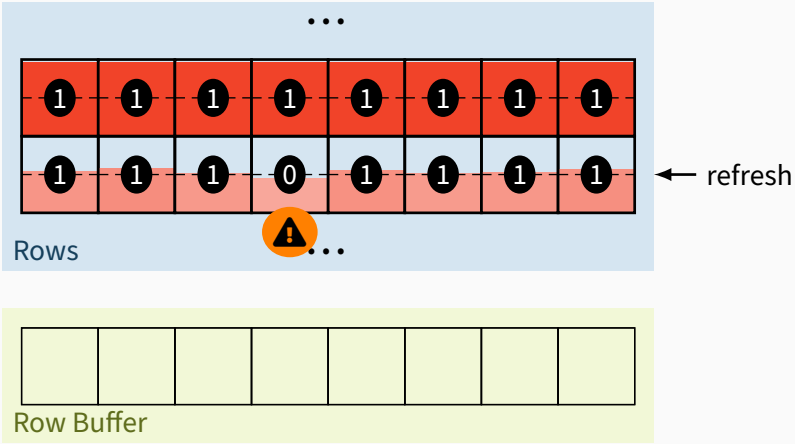

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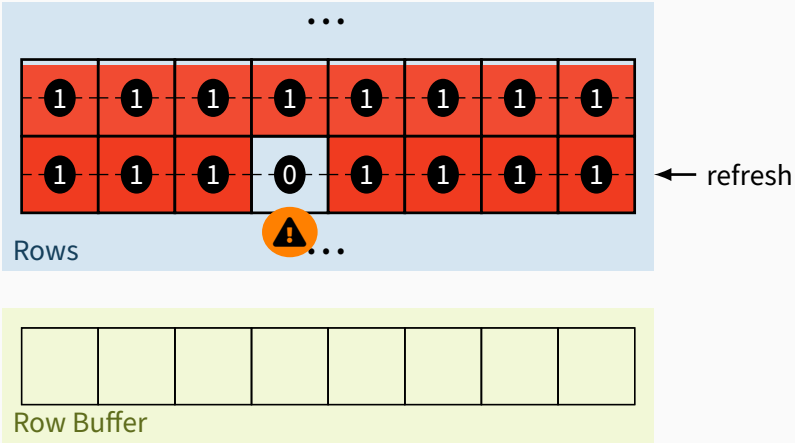
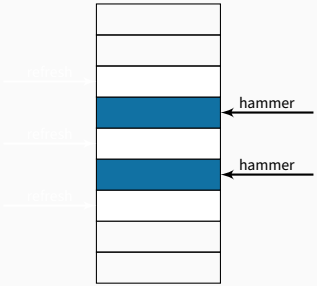


Target Row Refresh (TRR)



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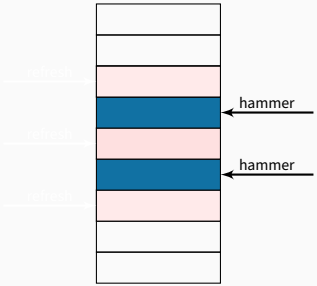

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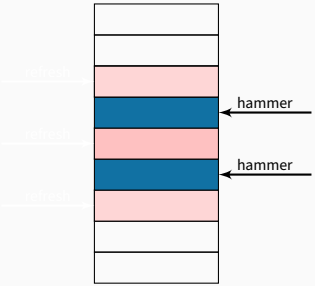

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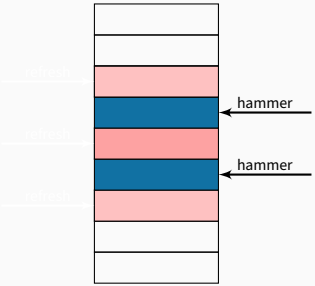

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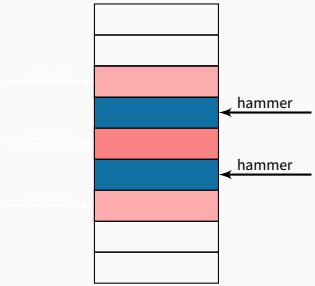

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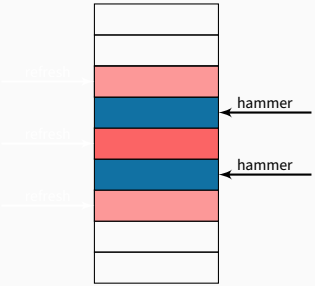

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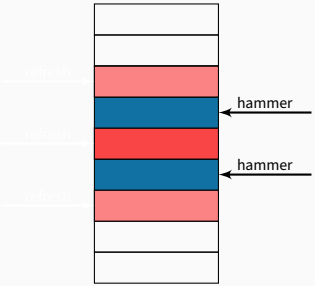

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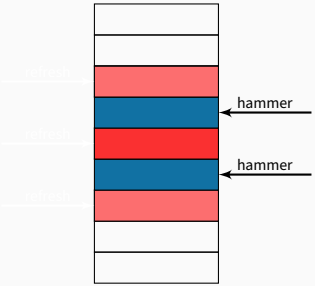

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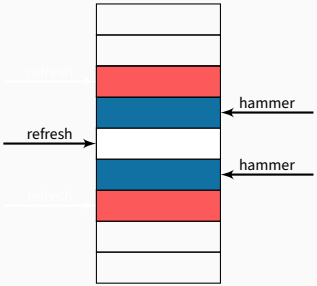

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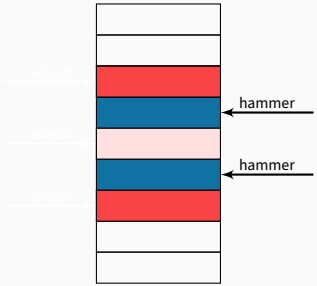

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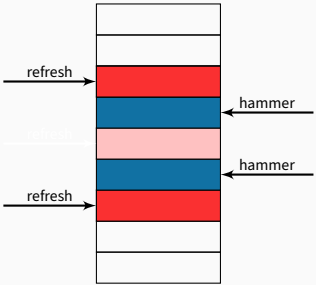

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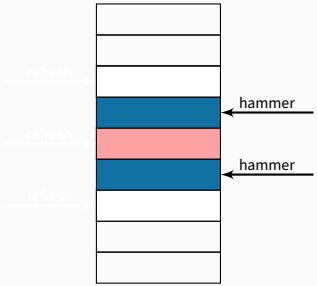

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- Not deployed in practice
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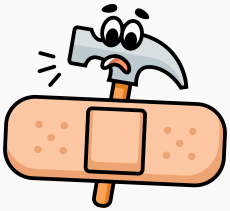
- $\rightarrow$ modern and future systems may still be vulnerable



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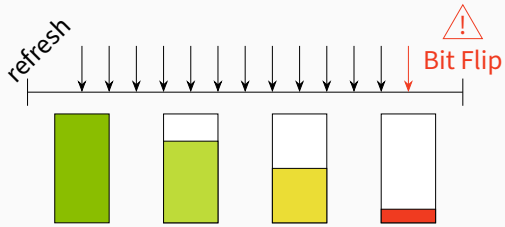
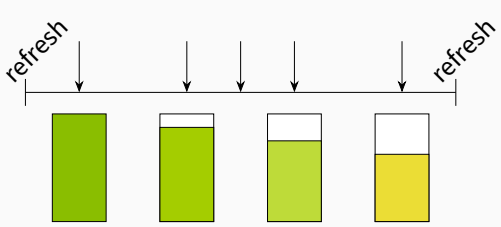
- Addressing functions distribute accesses across banks
- Attacks circumventing TRR need many accesses **per bank**
- $\rightarrow$ limit bandwidth per bank

Per-Bank Bandwidth Limit



unrestricted

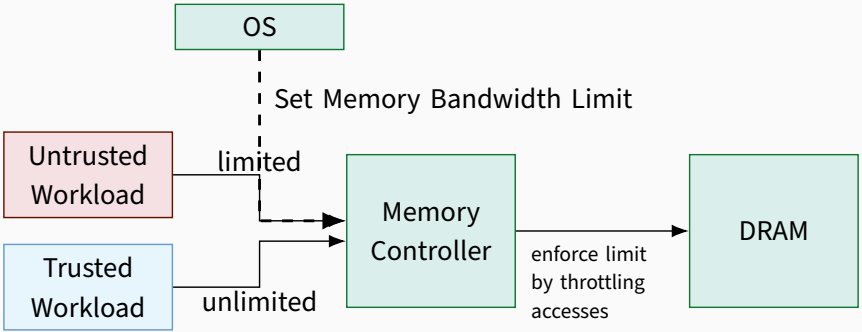


rate-limited

Mitigation Criteria

- Prevent bit flips
- Maintain performance
- Configurability

Memory Band-Aid



How does the Memory Controller know?

Quality-of-Service Features

- Monitor and restrict cache and memory utilization

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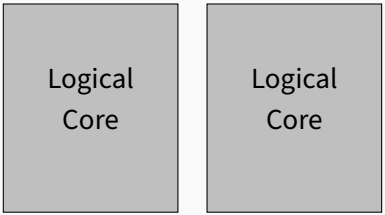
- AMD: L3 External Bandwidth Enforcement (L3BE)
  - 128 $\mathrm{MiB/s}$ increments
- Intel: Memory Bandwidth Allocation (MBA)
  - 10 % of system bandwidth increments

Class of Service (COS)



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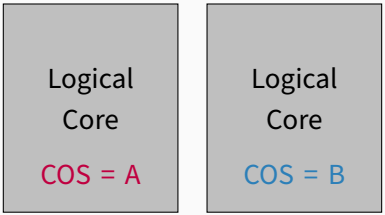

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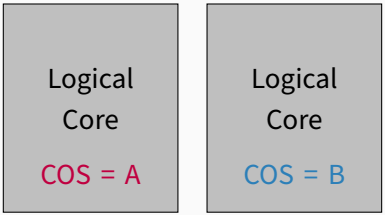

COS	Bandwidth Limit
A	restricted
B	unlimited

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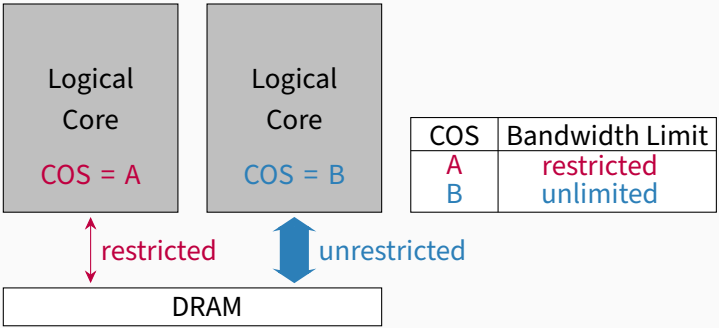
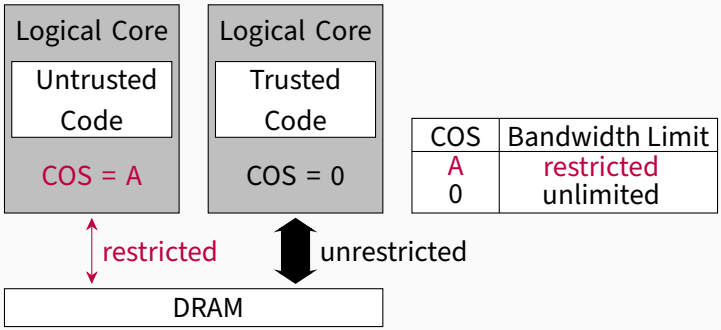


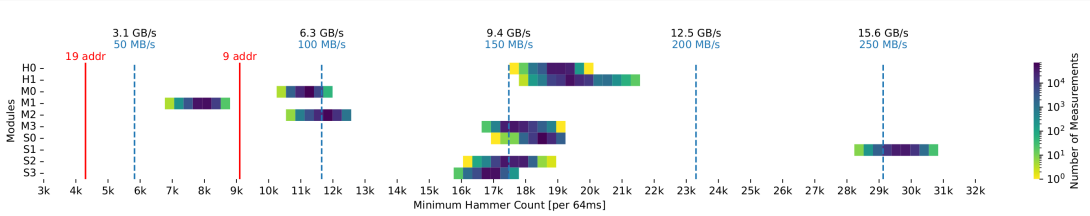
Proof-of-Concept Implementation



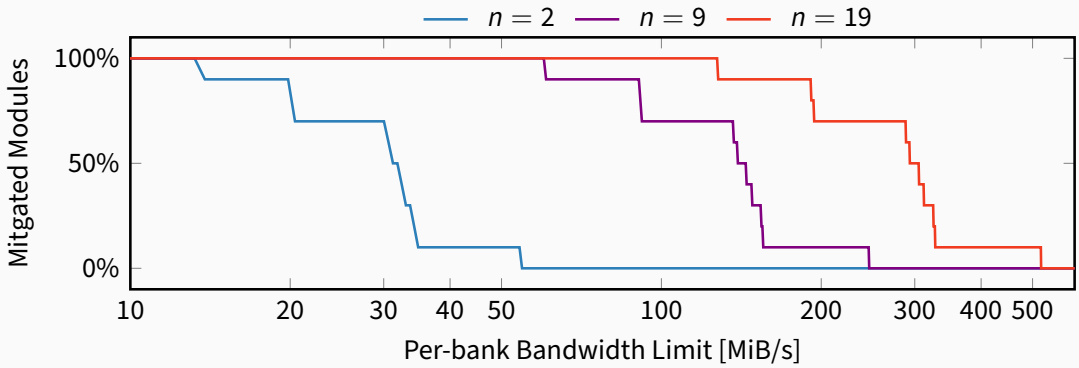
- OS sets COS on context switch: restricted = untrusted vs unrestricted = trusted
- Sandboxes or userspace vs kernelspace

What are suitable limits?

Minimum Hammer Counts



Mitigated Modules



Evaluation

Test Systems

Abbreviation	Processor	OS	DRAM Vendor	DRAM Speed	Configuration	Ranks	Total Banks	ECC	MBA/L3BE
A1	AMD Ryzen 7700X	Ubuntu 22.04	Kingston	DDR5	$2 \times$ 16GB	1	64	✗	✓
A2	AMD Epyc 8024P	Ubuntu 22.04		4800	$3 \times$ 16GB	1	96	✓	✓
I1	Intel Xeon 4514Y	Ubuntu 24.04		MT/s	$8 \times$ 16GB	1	256	✓	✓
I2	Intel Xeon 4410T	Ubuntu 22.04		62.7 $\mathrm{GiB/s}$	$4 \times$ 16GB	1	128	✓	✓

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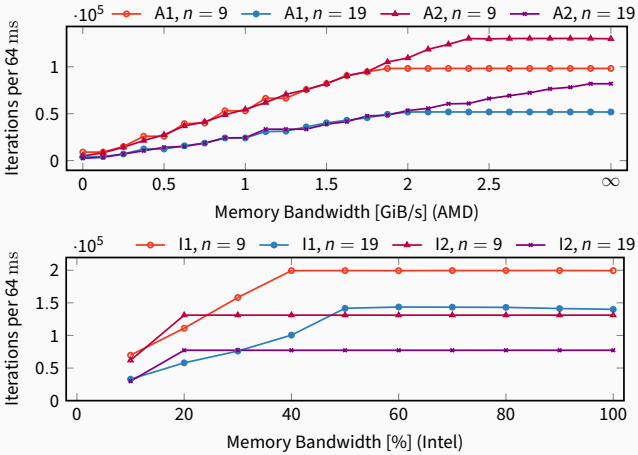
- Per-core limits

Are available limits secure?

Flush+Reload Iteration Limits



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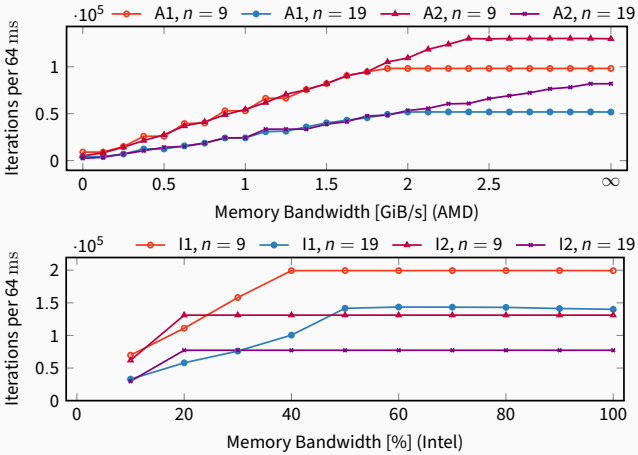
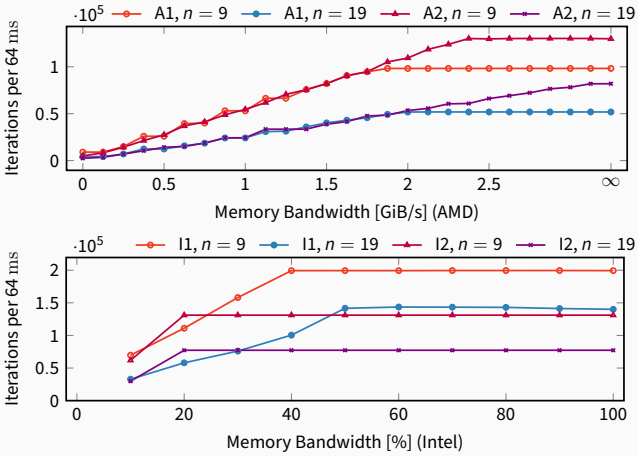


- ☑ AMD: prevent many-sided attacks

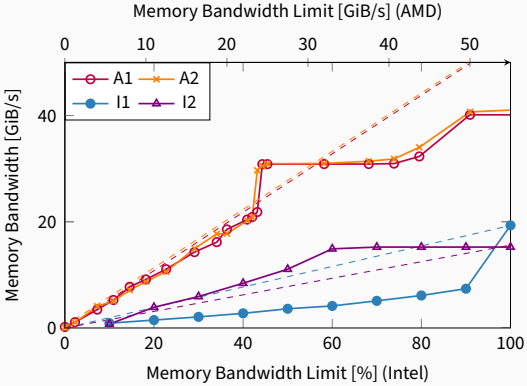
Flush+Reload Iteration Limits



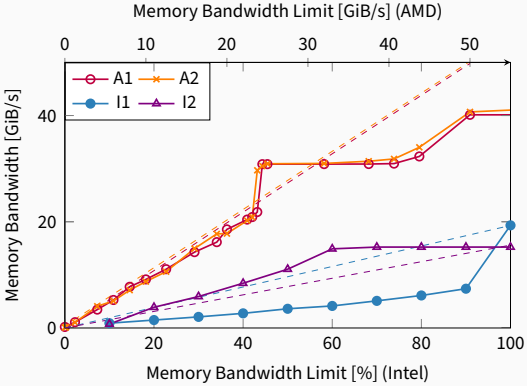
- ☑ AMD: prevent many-sided attacks
- ✗ Intel: insufficient limits

What is the performance impact?

Memory Sweep

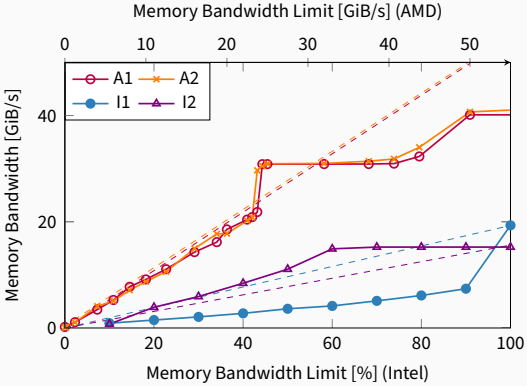


Memory Sweep



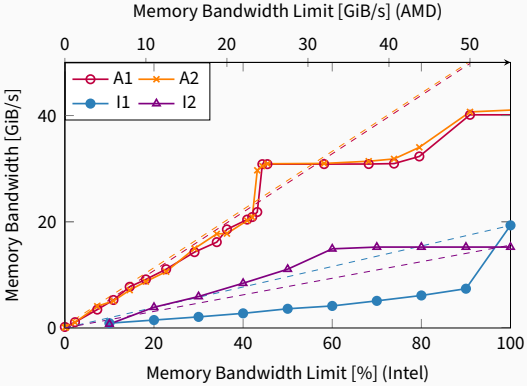
☑ Necessary slow-down

Memory Sweep



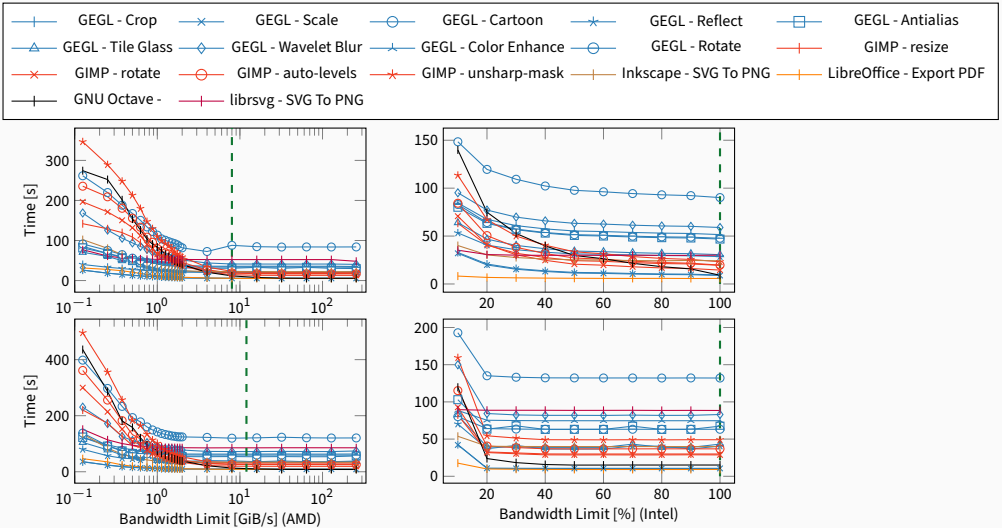
- ☑ Necessary slow-down
- ✗ Lack of adherence to limit

Memory Sweep

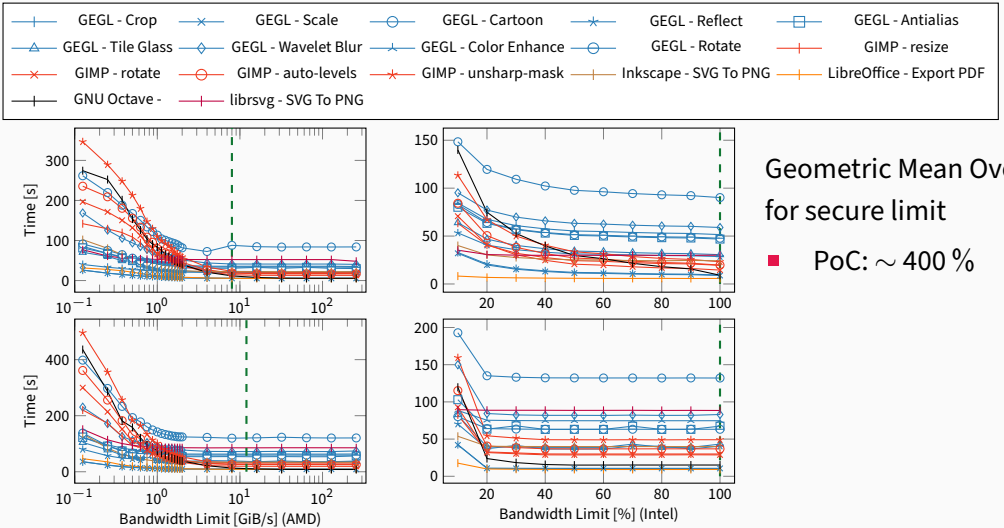


- ☑ Necessary slow-down
- ✗ Lack of adherence to limit
- ⚠ Wasted performance

Phoronix Productivity Testsuite



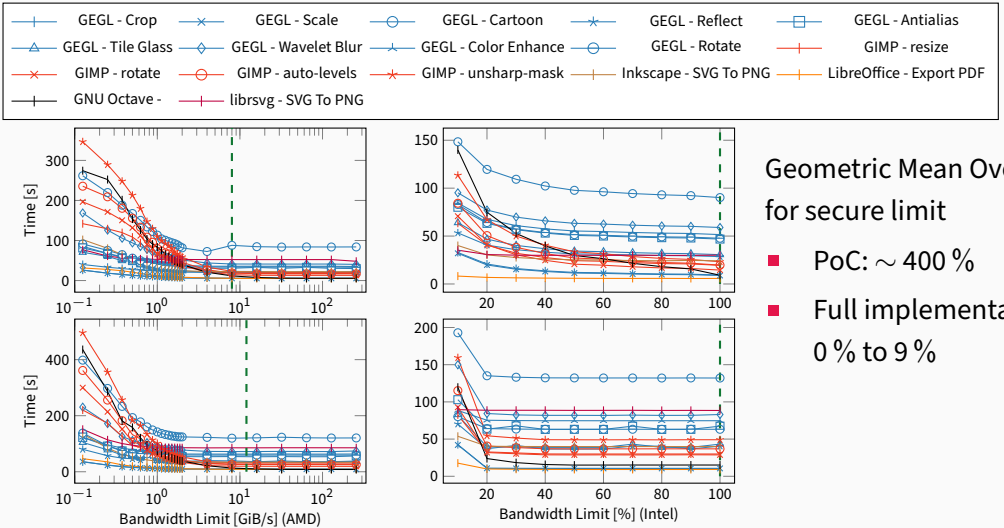
Phoronix Productivity Testsuite



Geometric Mean Overhead for secure limit

- PoC: $\sim 400\,\%$

Phoronix Productivity Testsuite

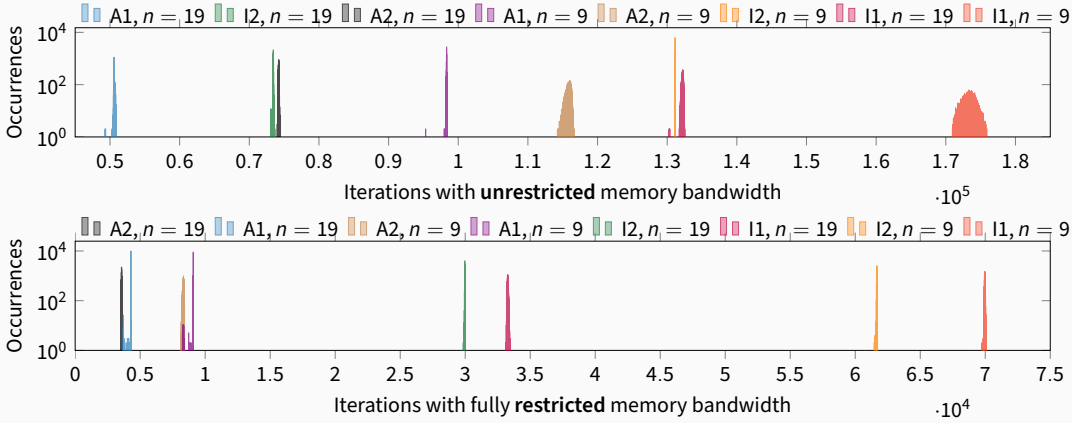


Geometric Mean Overhead for secure limit

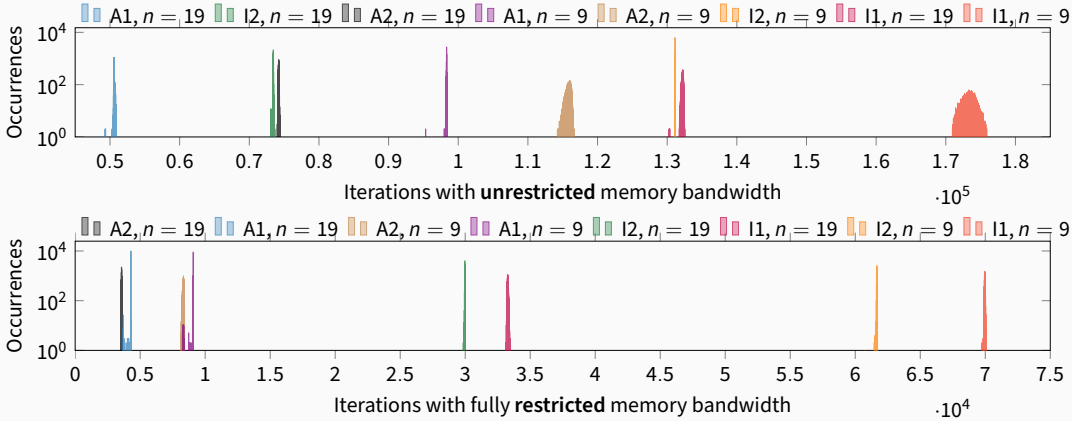
- PoC: $\sim 400\,\%$
- Full implementation: $0\,\%$ to $9\,\%$

How tightly are the limits adhered to?

Limit Consistency: Flush+Reload Iterations per 64 ms

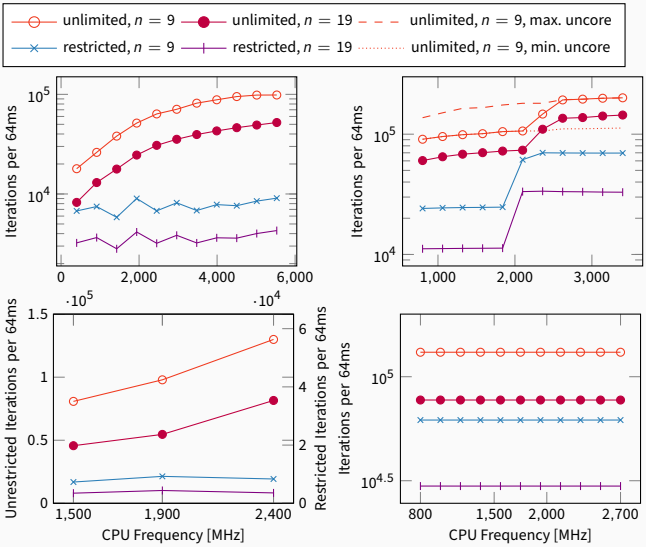


Limit Consistency: Flush+Reload Iterations per 64 ms

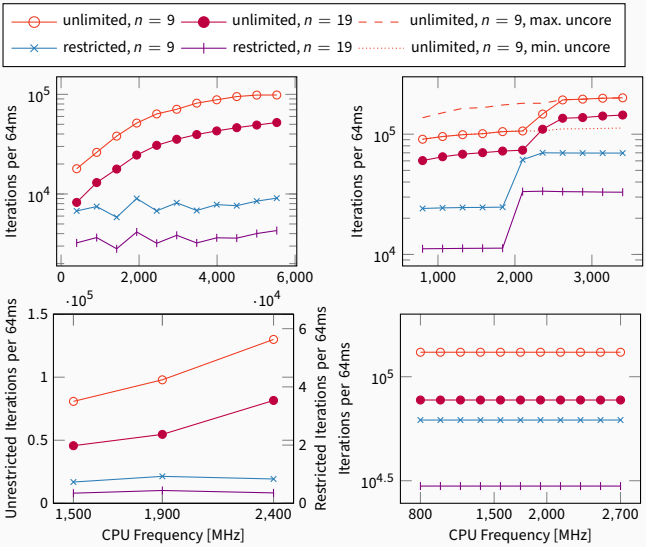


☑ Secure, but some performance loss

Frequency Impact

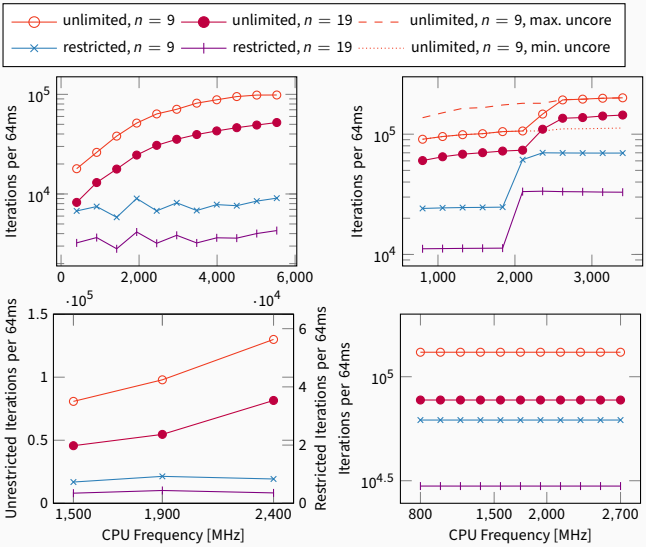


Frequency Impact



- CPU frequency can influence limit
- e.g. indirectly via uncore frequency

Frequency Impact



- ⚠ CPU frequency can influence limit
- ⚠ e.g. indirectly via uncore frequency
- ☑ Measurements already taken with maximum frequency

Memory Band-Aid Summary

- ☑ Effective defense against many-sided attacks
- ☑ Acceptable performance overhead
- ⚠ Current hardware support limited

Acknowledgments

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Memory Band-Aid

A Principled Rowhammer Defense-in-Depth

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